NSM-9DX Series Transceivers

Troubleshooting Instructions

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NSM-9DX Series Transceivers

Baseband Troubleshooting Instructions

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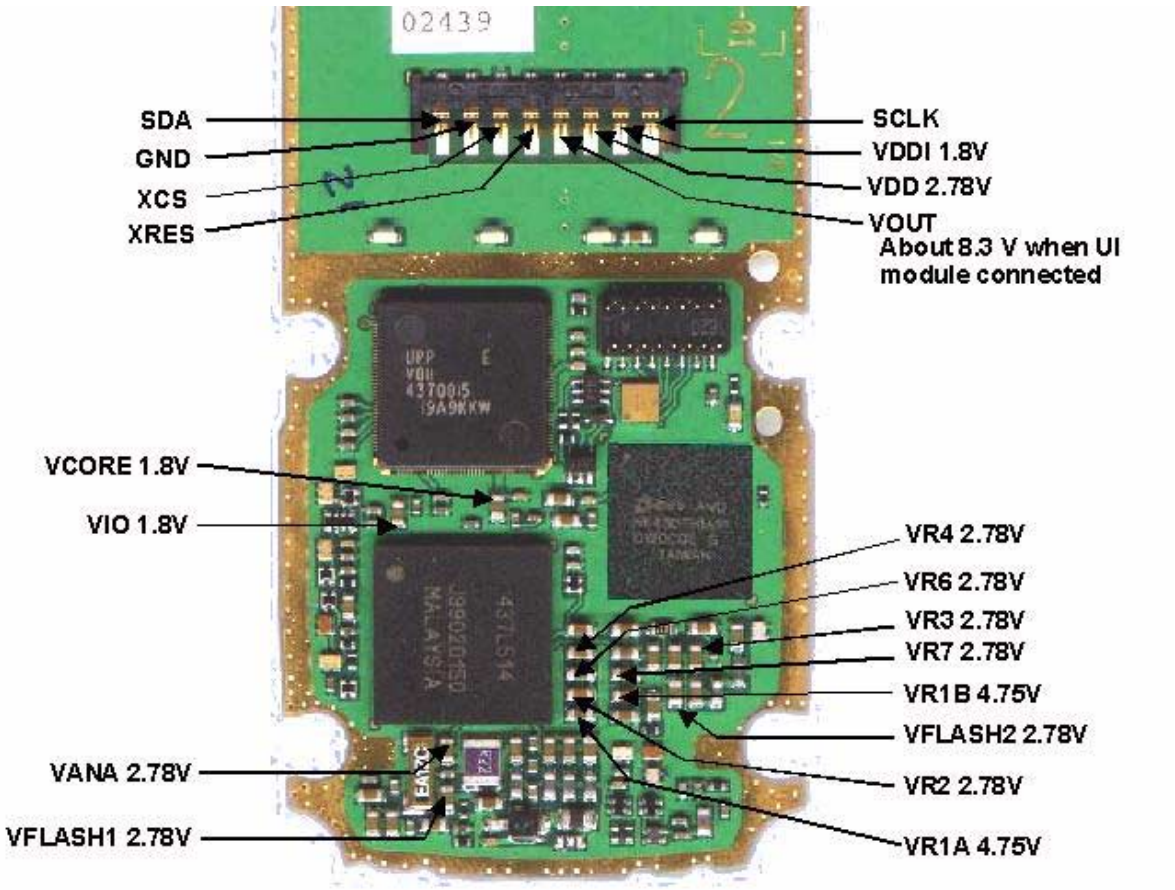
PWB Points (and Measurement Points)

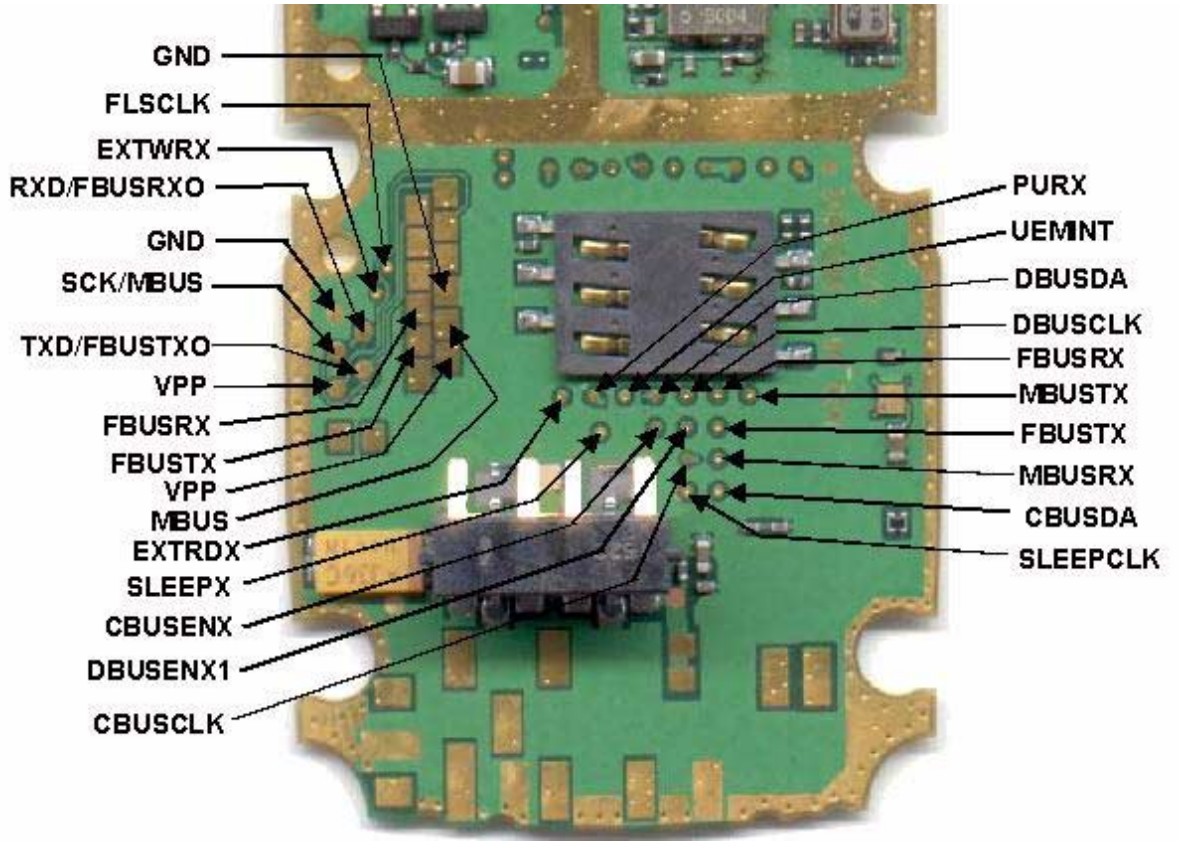
The following figures are the most needed test points in the NSM-9DX transceiver.

Figure 1: Picture of top test points



See FM Radio Troubleshooting for information on FM-radio.

Figure 2: Picture of bottom test points



Note! For test point pictures with references, see section Schematic Diagrams pages 19 and 20 for pictures of both Top test points and Bottom test points.

Table 1: Test points

REFERENCE	SIGNAL	NOTE
C205	VFLASH1	2.78 V regulator output UEM (D200) -> external FLASH memory
C204	VFLASH2	2.78V regulator output UEM (D200) -> FM Radio
C206	VANA	2.78 V regulator output UEM (D200) -> internal and external analog circuitry
C207	VIO	1.8 V regulator output UEM (D200) -> internal and external logic circuitry
C208	VCORE	1.8 V programmable regulator output UEM (D200) -> UPP (D400)
C221	VR1A	4.75 V RF regulator output UEM (D200) -> HAGAR (N600)
C222	VR4	2.78 V regulator output UEM (D200) -> HAGAR (N600)

C223	VR6	2.78 V regulator output UEM (D200) -> HAGAR (N600)
C224	VR7	2.78 V regulator output UEM (D200) -> VCO (G650)
C225	VR2	2.78 V regulator output UEM (D200) -> transf balun (T700)
C227	VR3	2.78 V regulator output UEM (D200) -> HAGAR (N600) and VCTCXO (G660)
C660	RFCLK (26MHz)	Main clock oscillator 26 MHz, **see Figure 3, "C660: RFCLK (26 MHz), VCTCXO (G660 pin 3) -> HAGAR (N600 pin H1)," on page 13** VCTCXO (G660) -> HAGAR (N600)
J1	RESET	Reset signal, **see Figure 4, "J1: RESET, UPP (D400 pin D12) -> HAGAR (N600 pin E3)," on page 13** UPP (D400) -> HAGAR (N600)
J2	RFBUSDA	RFBUS data, **see Figure 5, "J2: RFBUSDA, UPP (D400 pin F12) -> HAGAR (N600 pin E1)," on page 14** UPP (D400) -> HAGAR (N600)
J3	RFBUSCLK	RFBUS clock, **see Figure 6, "J3: RFBUSCLK, UPP (D400 pin G11) -> HAGAR (N600 pin E2)," on page 14 and Figure 7, "J3: RFBUSCLK (closer look), UPP (D400 pin G11) -> HAGAR (N600 pin E2)," on page 15** UPP (D400) -> HAGAR (N600)
J4	RFBUSEN1	RFBUS enable, **see Figure 8, "J4: RFBUSEN1, UPP (D400 pin G13) -> HAGAR (N600 pin D1)," on page 15** UPP (D400) -> HAGAR (N600)
J100	VBAT	Battery voltage pad for jig
J101	BSI	Battery size indicator for jig
J102	BTEMP	Battery temperature for jig
J386	SIMDATA	SIM data, **see** Figure 9, "J386: SIMDATA, UEM (D200 pin B2) <-> SIM CARD READER (X386 pin 4," on page 16 UEM (D200) <-> SIM CARD READER (X386)
J387	SIMRST	SIM reset, **see Figure 10, "J387: SIMRST, UEM (D200 pin A2) <-> SIM CARD READER (X386 pin 2)," on page 16** UEM (D200) -> SIM CARD READER (X386)
J388	SIMCLK	SIM clock, **see Figure 11, "J388: SIMCLK, UEM (D200 pin B3) <-> SIM CARD READER (X386 pin 3)," on page 17** UEM (D200) -> SIM CARD READER (X386)
J389	VSIM	SIM voltage 3 V or 1.8 V UEM (D200) -> SIM CARD READER (X386)
J396 PAD 2	FBUSTX	FBUS transmitted data, **see Figure 12, "J396 PAD 2: FBUSTX (during flashing), UEM (D200 pin N5) -> SERVICE INTERFACE (J396 PAD 2)," on page 17** (during flashing) UEM (D200) -> SERVICE INTERFACE

J396 PAD 3	FBUSRX	FBUS received data, **see Figure 13, "J396 PAD 3 FBUSRX (during flashing), SERVICE INTERFACE (J396 PAD 3) -> UEM (D200 pin P5)," on page 18** (during flashing) SERVICE INTERFACE -> UEM (D200)
J396 PAD 6	VPP	Flash programming voltage UEM (D200), SERVICE INTERFACE -> FLASH (D450)
J396 PAD 7	MBUS	One wire bidirectional serial bus, **see Figure 14, "J396 PAD 7: MBUS (during flashing), UEM (D200 pin M6) <-> SERVICE INTERFACE (J396 PAD 7)," on page 18** (during flashing) UEM (D200) <-> SERVICE INTERFACE
J396 PAD 8	GND	Ground point for service interface
J402	PURX	Power Up Reset, **see Figure 15, "J402: PURX, UEM (D200 pin C10) -> UPP (D400 pin K2)," on page 19** UEM (D200) -> UPP (D400)
J403	SLEEPX	Sleep enable, **see Figure 16, "J403: SLEEPX, UEM (D200 pin B11) -> UPP (D400 pin L1)," on page 19** UEM (D200) -> UPP (D400)
J404	SLEEPCLK	Sleep clock, **see Figure 17, "J404: SLEEPCLK, UEM (D200 pin D9) -> UPP (D400 pin H3)," on page 20** UEM (D200) -> UPP (D400)
J405	UEMINT	UEM interrupt, **see Figure 18, "J405: UEMINT, UEM (D200 pin A10) -> UPP (D400 pin J2)," on page 20** UEM (D200) -> UPP (D400)
J406	CBUSCLK	CBUS clock, **see Figure 19, "J406: CBUSCLK, UEM (D200 pin A8) -> UPP (D400 pin G1)," on page 21** UEM (D200) -> UPP (D400)
J407	CBUSDA	CBUS data, **see Figure 20, "J407: CBUSDA, UEM (D200 pin B7) <-> UPP (D400 pin G2)," on page 21** UEM (D200) <-> UPP (D400)
J408	CBUSENX	CBUS enable, **see Figure 21, "J408: CBUSENX, UEM (D200 pin C8) -> UPP (D400 pin F3)," on page 22** UEM (D200) -> UPP (D400)
J409	MBUSTX	MBUS transmitted data, **see Figure 22, "J409: MBUSTX (during flashing), UPP (D400 pin E3) -> UEM (D200 pin C6)," on page 22** (during flashing) UPP (D400) -> UEM (D200)
J410	MBUSRX	MBUS received data, **see Figure 23, "J410: MBUSRX (during flashing), UEM (D200 pin D6) -> UPP (D400 pin D3)," on page 23** (during flashing) UEM (D200) -> UPP (D400)
J411	FBUSTX	FBUS transmitted data, **see Figure 24, "J411: FBUSTX (during flashing), UPP (D400 pin F1) -> UEM (D200 pin A7)," on page 23** (during flashing) UPP (D400) -> UEM (D200)
J412	FBUSRX	FBUS received data, **see Figure 25, "J412: FBUSRX (during flashing), UEM (D200 pin C7) -> UPP (D400 pin E4)," on page 24** (during flashing) UEM (D200) -> UPP (D400)

J413	DBUSCLK	DBUS clock, **see Figure 26, "J413: DBUSCLK, UEM (D200 pin D10) -> UPP (D400 pin K3)," on page 24** UEM (D200) -> UPP (D400)
J414	DBUSDA	DBUS data, **see Figure 27, "J414: DBUSDA, UEM (D200 pin A11) <-> UPP (D400 pin L3)," on page 25** UEM (D200) <-> UPP (D400)
J415	DBUSENX1	DBUS enable, **see Figure 28, "J415: DBUSENX1, UEM (D200 pin B10) -> UPP (D400 pin J3)," on page 25** UEM (D200) -> UPP (D400)
J416	EXTWRX	FLASH write enable, **see Figure 29, "J416: EXTWRX (during flashing), UPP (D400 pin N9) -> FLASH (D450 pin A6)," on page 26** (during flashing) UPP (D400) -> FLASH (D450)
J417	EXTRDX	FLASH read enable, **see Figure 30, "J417: EXTRDX, UPP (D400 pin L7) -> FLASH (D450 pin C10)," on page 26** UPP (D400) -> FLASH (D450)
J418	FLS2CSX	UPP (D400) -> TESTPOINT
J419	FLSCLK	FLASH clock, **see Figure 31, "J419: FLSCLK, UPP (D400 pin N12) -> FLASH (D450 pin A4)," on page 27** UPP (D400) -> FLASH (D450)
J420	FLSCSX	FLASH chip enable, **see Figure 32, "J420: FLSCSX, UPP (D400 pin N6) -> FLASH (D450 pin B9)," on page 27** UPP (D400) -> FLASH (D450)
J470	VBAT	Battery voltage
J471	GENTEST0/ STITxD	OSTRICH transmitted data UPP (D400) -> TESTPOINT
J472	GENTEST1/ STISClk	OSTRICH clock UPP (D400) -> TESTPOINT
J473	STIRxD	OSTRICH received data UPP (D400) -> TESTPOINT
J474	GND	Ground point
J480	JTMS	UPP (D400) -> TESTPOINT
J481	JTRst	UPP (D400) -> TESTPOINT
J482	JTDI	UPP (D400) -> TESTPOINT
J483	VCC	Supply voltage from 1.8 V VIO regulator
J484	JTDO	UPP (D400) -> TESTPOINT
J485	JTClk_ret	UPP (D400) -> TESTPOINT
J486	JTClk	UPP (D400) -> TESTPOINT
J487	EMU0	UPP (D400) -> TESTPOINT
J488	EMU1	UPP (D400) -> TESTPOINT
J489	GND	Ground point

J700	TXP	Transmitted power control**, see Figure 33, "J700: TXP, UPP (D400 pin D11) -> HAGAR (N600 pin D5)," on page 28** (during call) UPP (D400) -> HAGAR (N600)
R301	PWRONX	Power on button, **see Figure 34, "R301: PWRONX, POWER BUTTON (S300) -> UEM (D200 pin P7)," on page 28** POWER BUTTON -> UEM (D200)
R305	KLIGHT	Backlight enable, **see Figure 35, "R305: KLIGHT, UEM (D200 pin F3) -> BACKLIGHT CIRCUITRY (V300 pins 2,3,5 and V301 pins 2,5,6)," on page 29** UEM (D200) -> BACKLIGHT CIRCUITRY (V300 and V301)
R420	RFCLK (13MHz)	Main clock 13 MHz, **see Figure 36, "R420: RFCLK (13 MHz), HAGAR (N600 pin E4) -> UPP (D400 pin M5)," on page 29** HAGAR (N600) -> UPP (D400)
X100 PIN 1	GND	Ground point
X100 PIN 2	VCHAR	Charger voltage SYSTEM CONNECTOR (X100) -> UEM (D200)
X100 PIN 3	XMICN	External mic (-) SYSTEM CONNECTOR (X100) -> UEM (D200)
X100 PIN 4	XEARN	External earpiece (-) SYSTEM CONNECTOR (X100) -> UEM (D200)
X100 PIN 5	XMICP	External mic (+) SYSTEM CONNECTOR (X100) -> UEM (D200)
X100 PIN 6	HEADINT	Headset interrupt SYSTEM CONNECTOR (X100) -> UEM (D200)
X100 PIN 7	XEARP	External earpiece (+) SYSTEM CONNECTOR (X100) -> UEM (D200)
X100 PIN 8	VBAT (VIBRA)	Vibra supply voltage VBAT -> SYSTEM CONNECTOR (X100)
X100 PIN 9	VIBRA	Vibra control, **see Figure 37, "X100 PIN 9: VIBRA, UEM (D200 pin G3) -> SYSTEM CONNECTOR (X100 pin 9)," on page 30** UEM (D200) -> SYSTEM CONNECTOR (X100)
X100 PIN 10	MIC (-)	Internal mic (-) SYSTEM CONNECTOR (X100) -> UEM (D200)
X100 PIN 11	MIC (+)	Internal mic (+) SYSTEM CONNECTOR (X100) -> UEM (D200)
X101 PIN 1	VBAT	Battery voltage BATTERY CONNECTOR (X101) -> VBAT
X101 PIN 2	BTEMP	Battery temperature BATTERY CONNECTOR (X101) -> UEM (D200)
X101 PIN 3	BSI	Battery size indicator BATTERY CONNECTOR (X101) -> UEM (D200)
X101 PIN 4	GND	Battery ground BATTERY CONNECTOR (X101) -> PHONE GROUND

X300 PIN 1	XRES	LCD reset, **see Figure 38, "X300 PIN 1: XRES (startup), UPP (D400 pin A7) -> LCD CONNECTOR (X300 pin 1)," on page 30** UPP (D400) -> LCD CONECTOR (X300)
X300 PIN 2	XCS	LCD chip select, **see Figure 39, "X300 PIN 2: XCS, UPP (D400 pin C7) -> LCD CONNECTOR (X300 pin 2)," on page 31** UPP (D400) -> LCD CONECTOR (X300)
X300 PIN 3	VSS	LCD ground LCD CONECTOR (X300) -> PHONE GROUND
X300 PIN 4	SDA	LCD data, **see Figure 40, "X300 PIN 4: SDA, UPP (D400 pin B6) -> LCD CONNECTOR (X300 pin 4)," on page 31** UPP (D400) -> LCD CONECTOR (X300)
X300 PIN 5	SCLK	LCD clock, **see Figure 41, "X300 PIN 5: SCLK, UPP (D400 pin C6) -> LCD CONNECTOR (X300 pin 5)," on page 32** UPP (D400) -> LCD CONECTOR (X300)
X300 PIN 6	VDDI	LCD logic voltage supply 1.8 V VIO 1.8 V -> LCD CONECTOR (X300)
X300 PIN 7	VDD	LCD voltage supply VFLASH1 2.78 V -> LCD CONECTOR (X300)
X300 PIN 8	VOUT	Booster output, **see Figure 42, "X300 PIN 8: VOUT, LCD CONNECTOR (X300 PIN 8) -> C301 and C302," on page 32** LCD CONNECTOR (X300) -> C301 and C302
X303 PIN 2	KEYB_LIGHT	Keyboard backlight current, **see Figure 43, "X303 PIN 2: KEYB_LIGHT, BACKLIGHT CIRCUITRY (V300 pin 6) -> UI CONNECTOR (X303 pin 2)," on page 33** BACKLIGHT CIRCUITRY (V300) -> UI CONNECTOR (X303)

Figure 3: C660: ***RFCLK*** (26 MHz), VCTCXO (G660 pin 3) -> HAGAR (N600 pin H1)

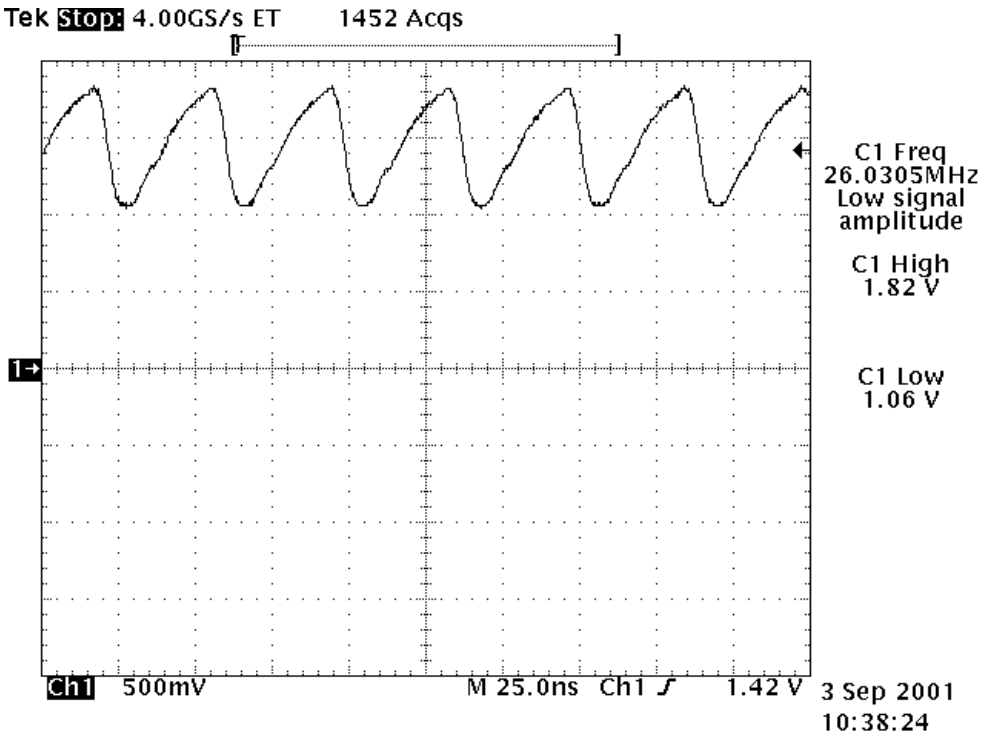


Figure 4: J1: ***RESET***, UPP (D400 pin D12) -> HAGAR (N600 pin E3)

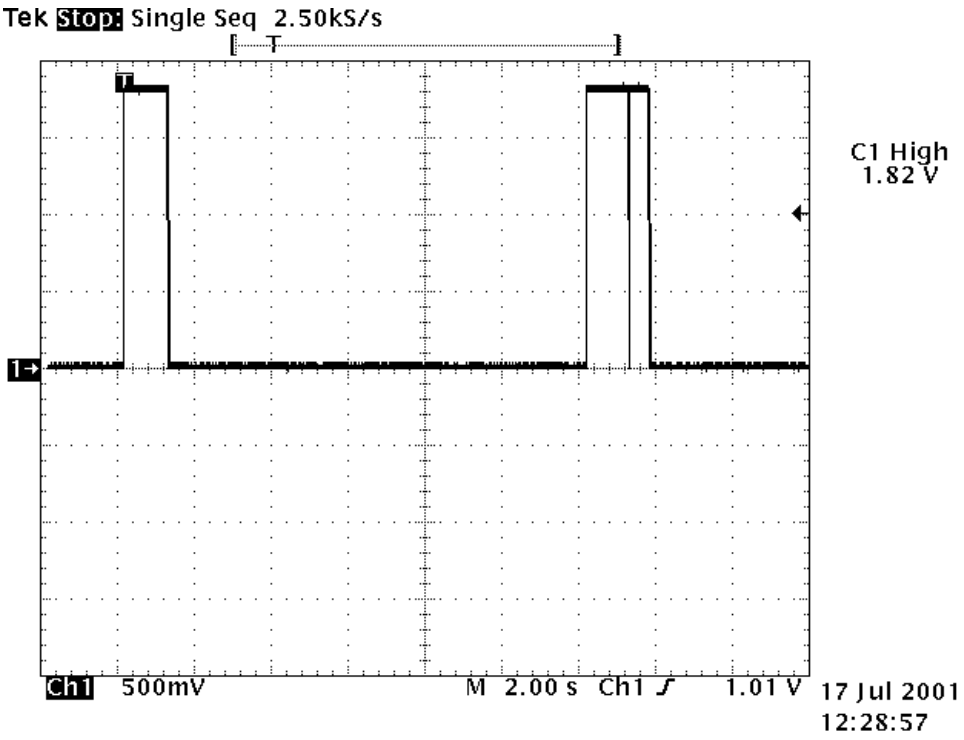


Figure 5: J2: ***RFBUSDA***, UPP (D400 pin F12) -> HAGAR (N600 pin E1)

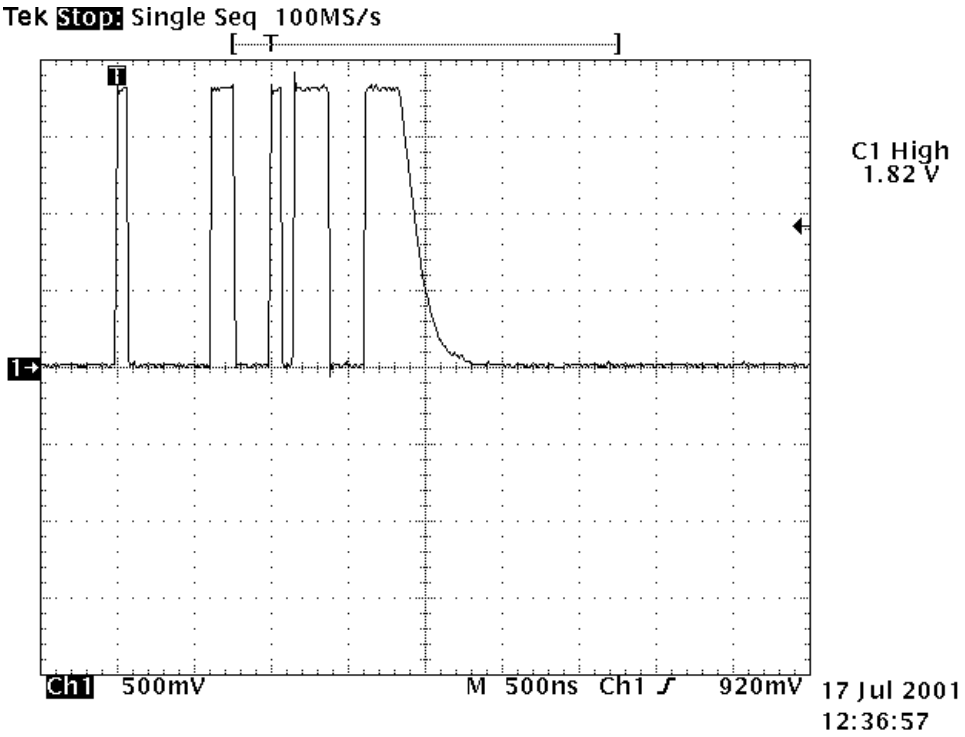


Figure 6: J3: ***RFBUSCLK***, UPP (D400 pin G11) -> HAGAR (N600 pin E2)

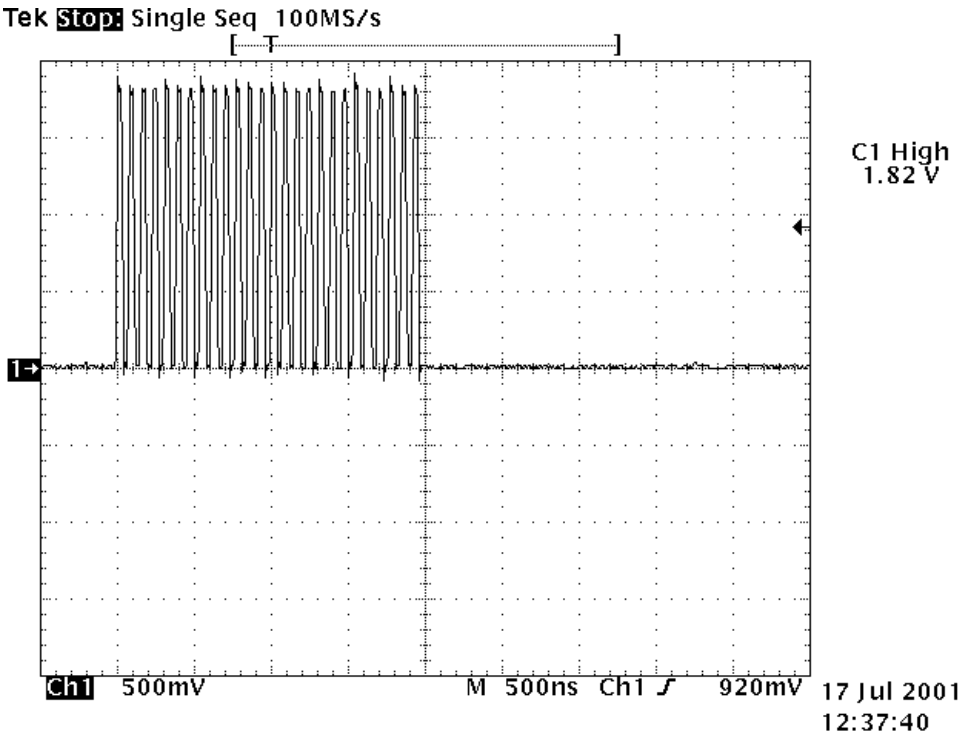


Figure 7: J3: ***RFBUSCLK*** (closer look), UPP (D400 pin G11) -> HAGAR (N600 pin E2)

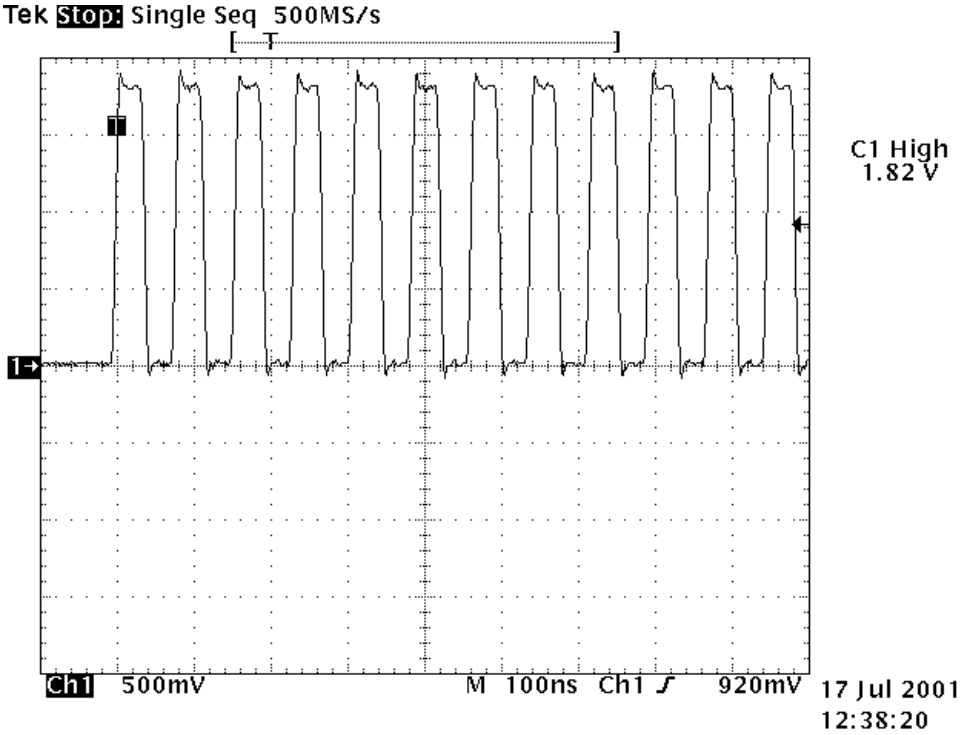


Figure 8: J4: ***RFBUSEN1***, UPP (D400 pin G13) -> HAGAR (N600 pin D1)

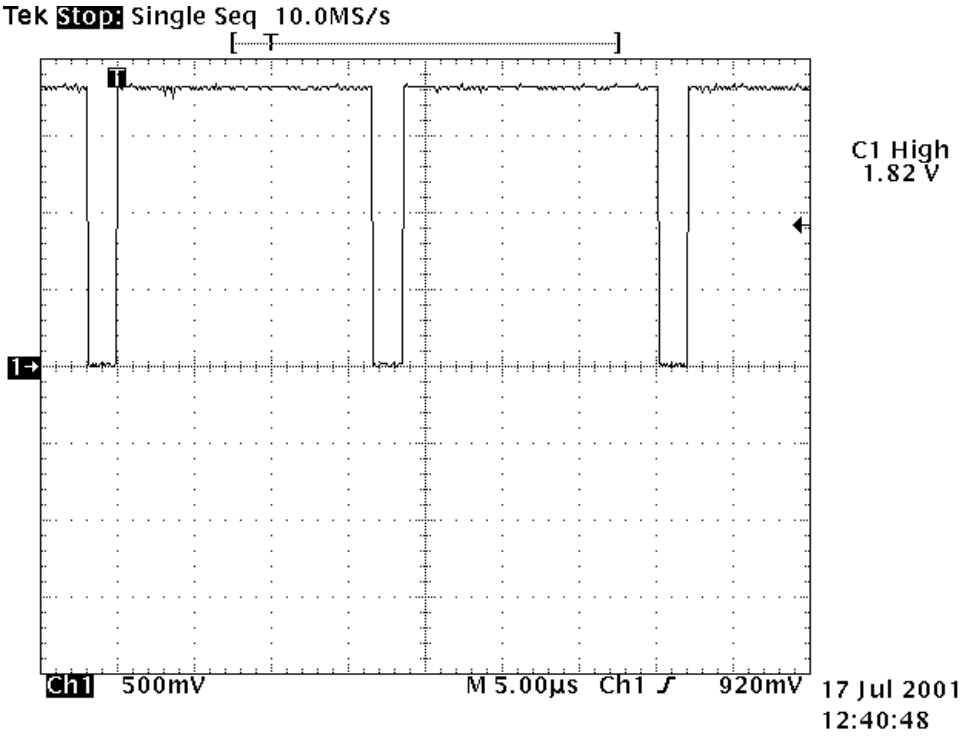


Figure 9: J386: ***SIMDATA***, UEM (D200 pin B2) <-> SIM CARD READER (X386 pin 4

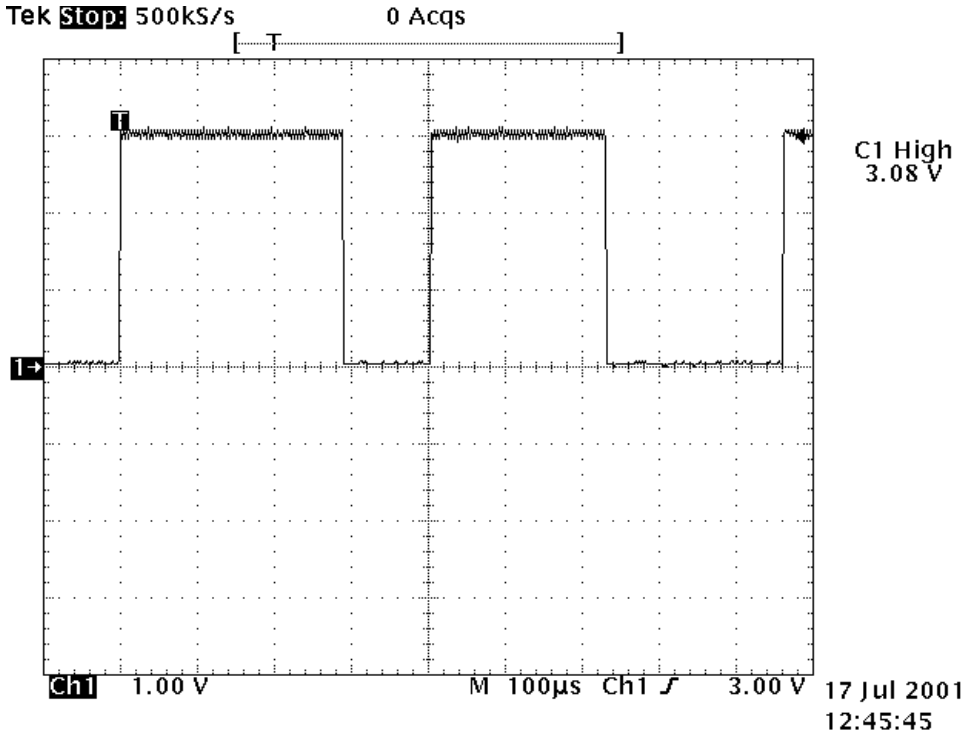


Figure 10: J387: ***SIMRST***, UEM (D200 pin A2) <-> SIM CARD READER (X386 pin 2)

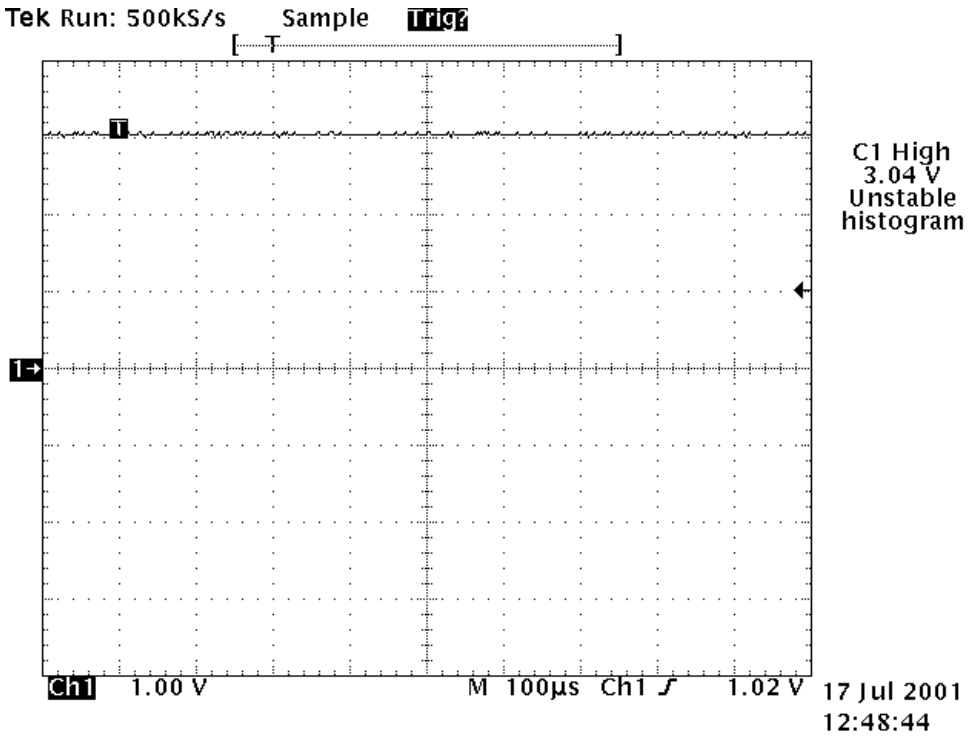


Figure 11: J388: ***SIMCLK***, UEM (D200 pin B3) <-> SIM CARD READER (X386 pin 3)

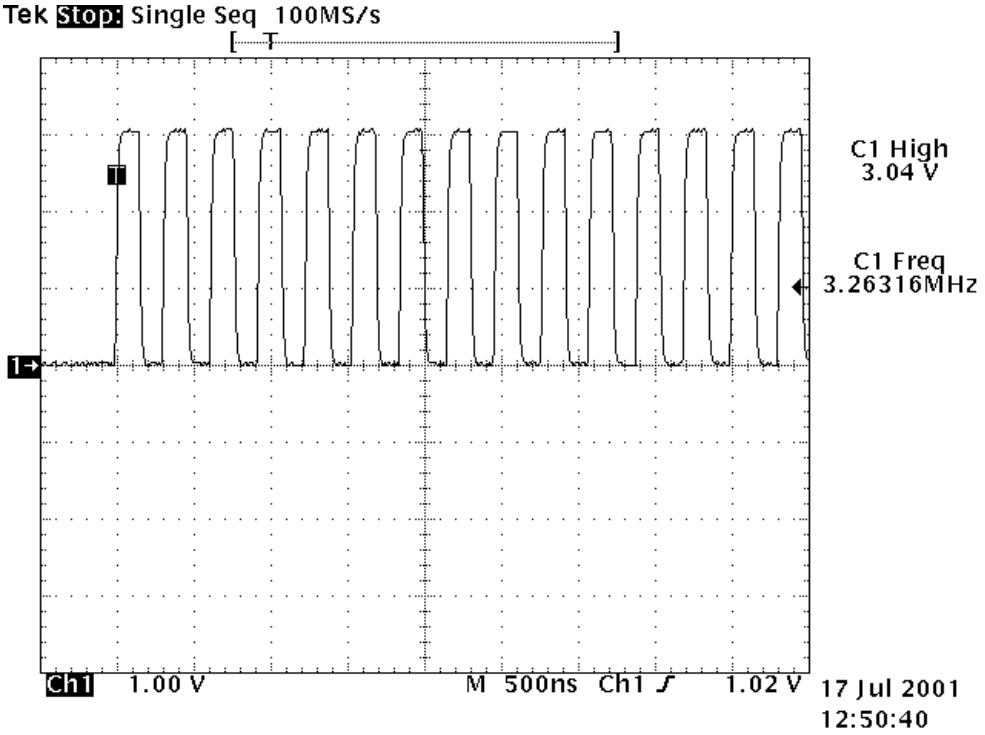


Figure 12: J396 PAD 2: ***FBUSTX*** (during flashing), UEM (D200 pin N5) -> SERVICE INTERFACE (J396 PAD 2)

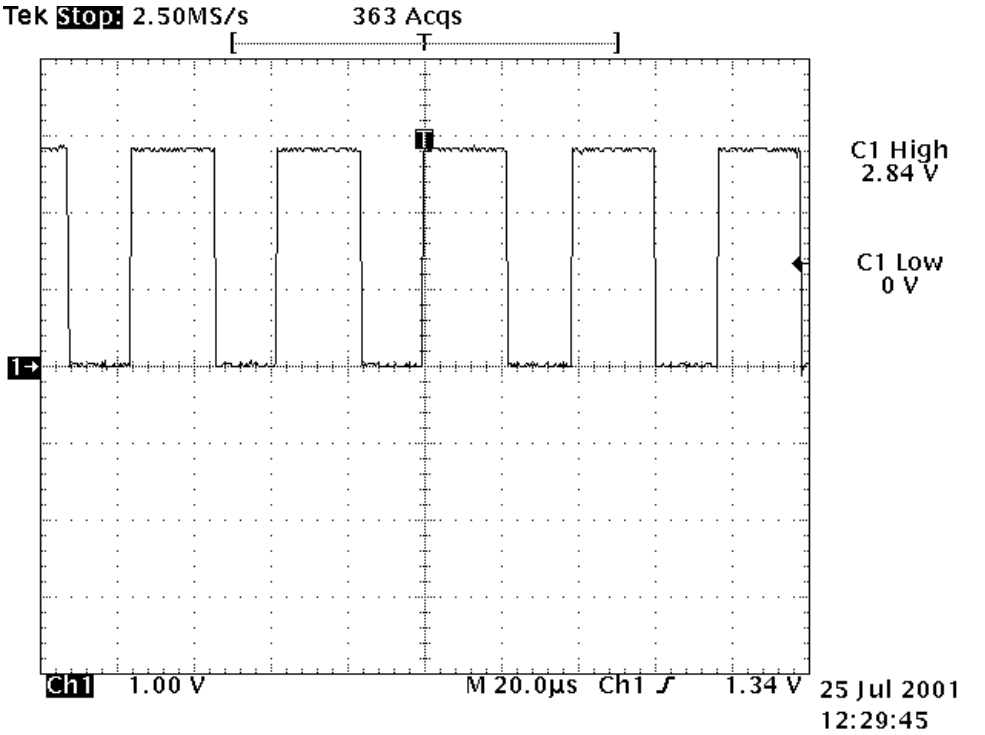


Figure 13: J396 PAD 3 ***FBUSRX*** (during flashing), SERVICE INTERFACE (J396 PAD 3) -> UEM (D200 pin P5)

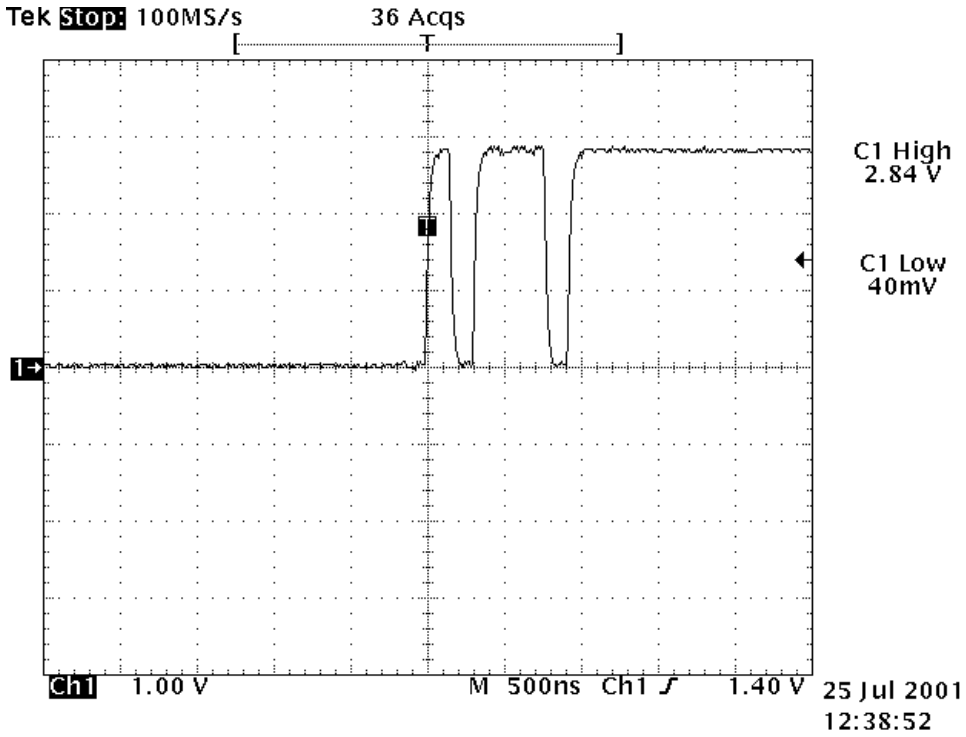


Figure 14: J396 PAD 7: ***MBUS*** (during flashing), UEM (D200 pin M6) <-> SERVICE INTERFACE (J396 PAD 7)

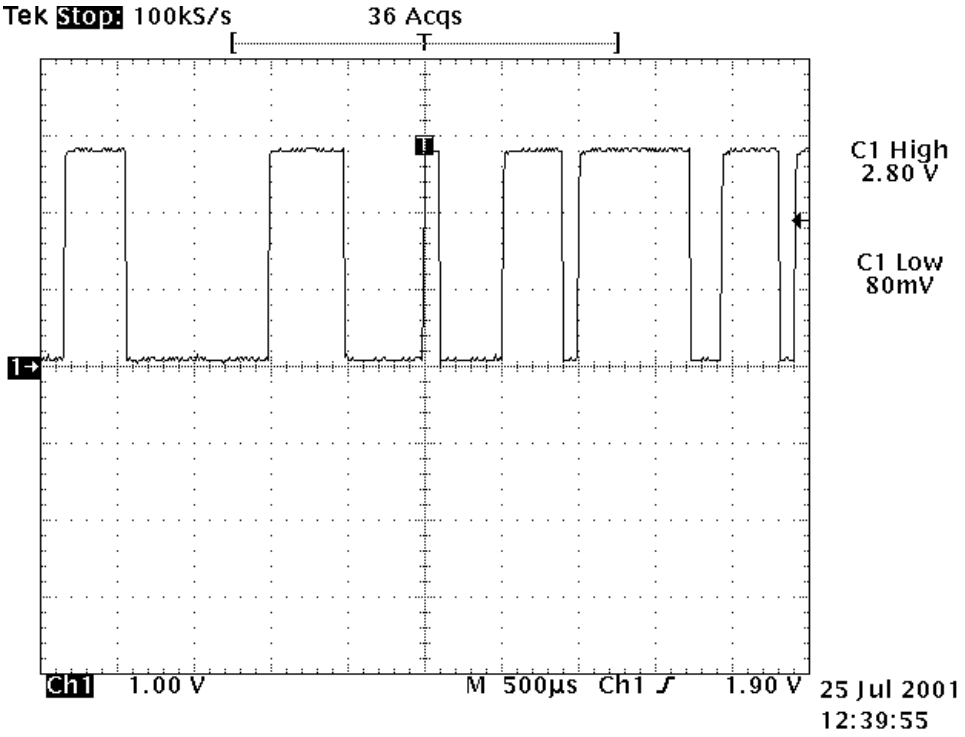


Figure 15: J402: ***PURX***, UEM (D200 pin C10) -> UPP (D400 pin K2)

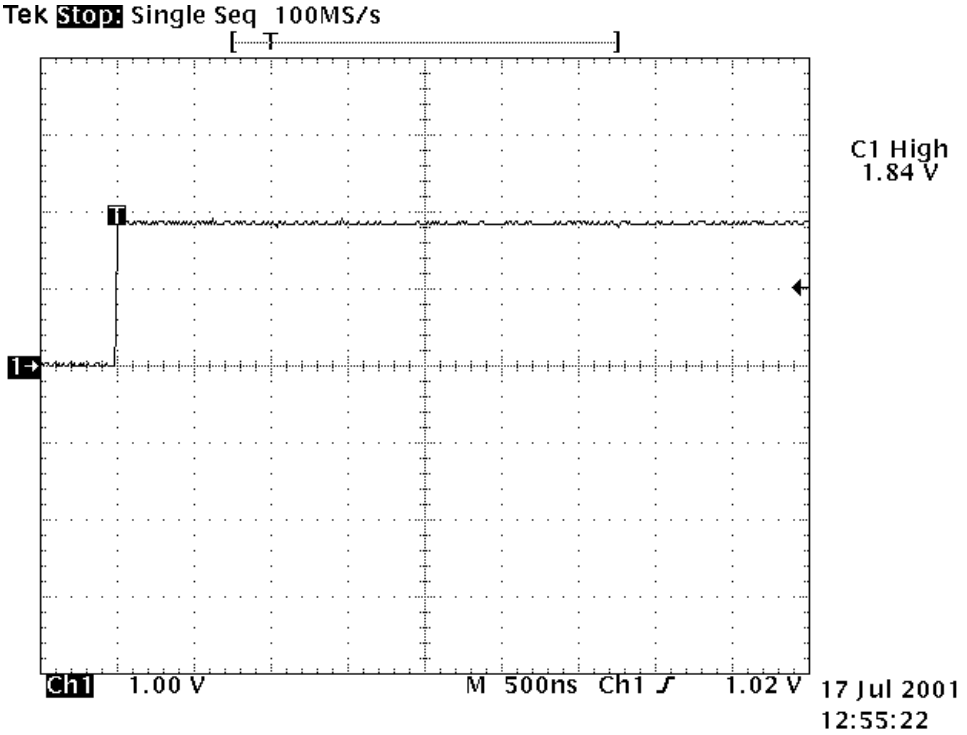


Figure 16: J403: ***SLEEPX***, UEM (D200 pin B11) -> UPP (D400 pin L1)

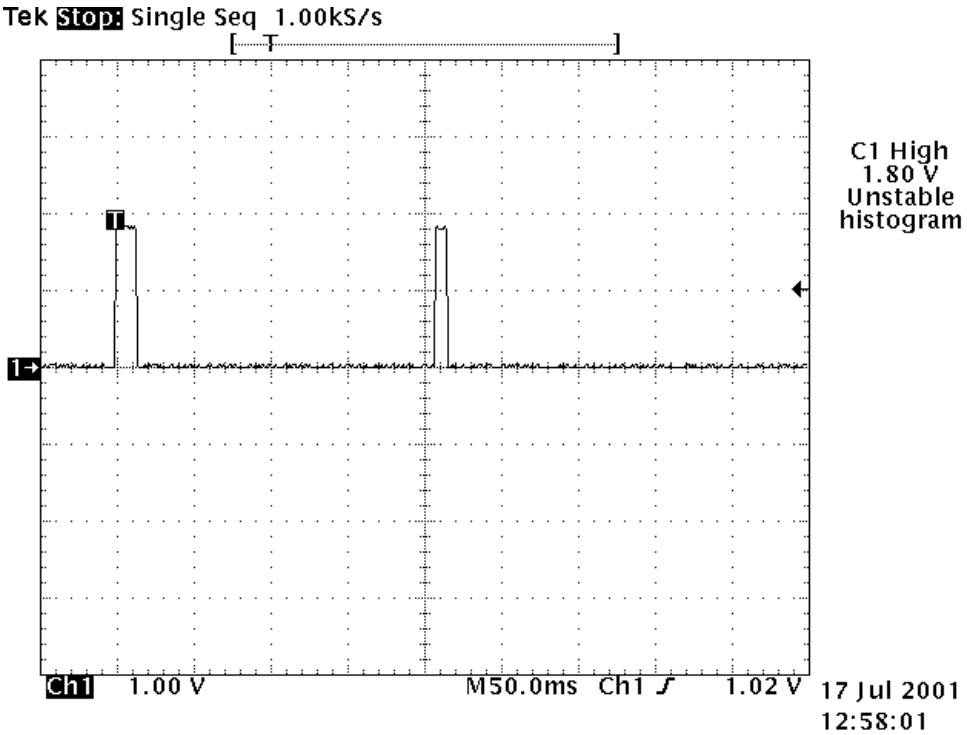


Figure 17: J404: ***SLEEPCLK***, UEM (D200 pin D9) -> UPP (D400 pin H3)

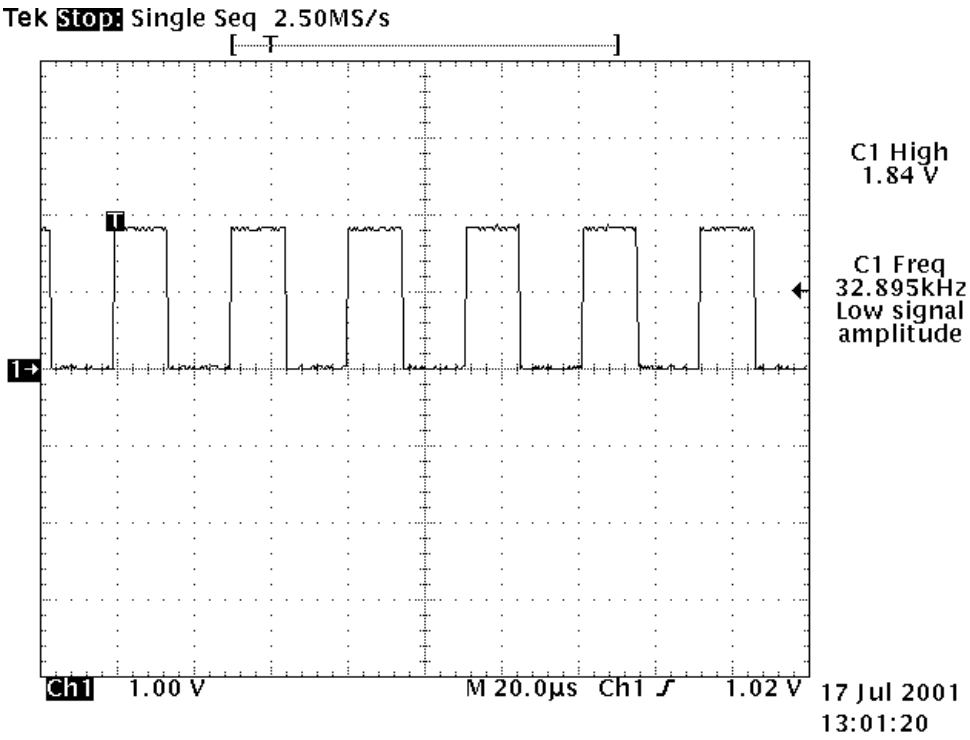


Figure 18: J405: ***UEMINT***, UEM (D200 pin A10) -> UPP (D400 pin J2)

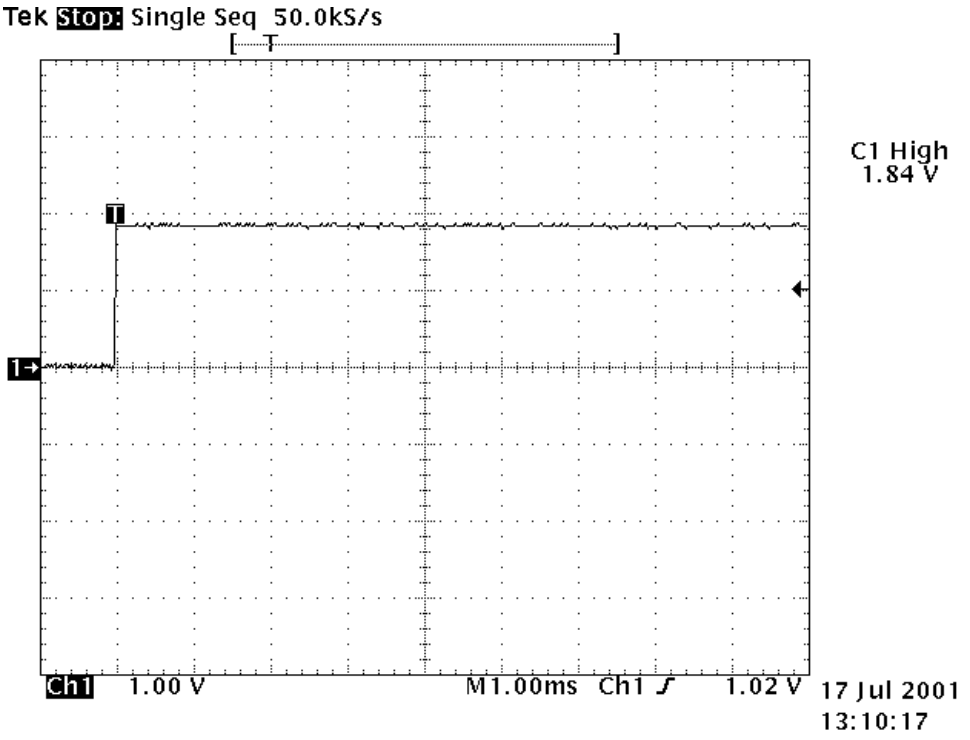


Figure 19: J406: ***CBUSCLK***, UEM (D200 pin A8) -> UPP (D400 pin G1)

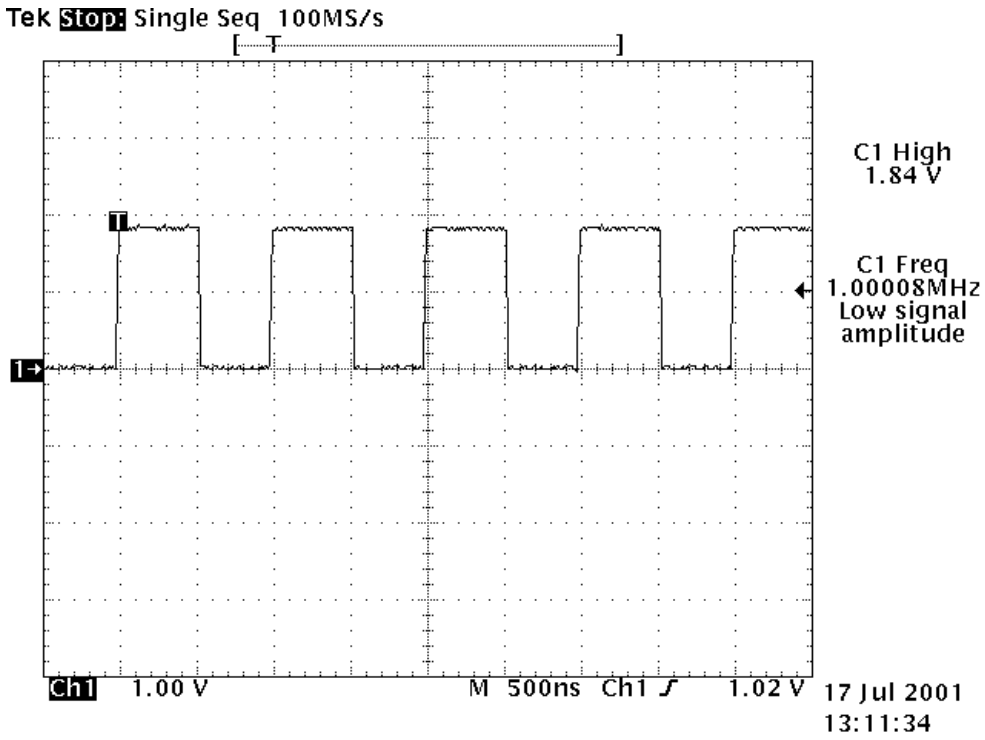


Figure 20: J407: ***CBUSDA***, UEM (D200 pin B7) <-> UPP (D400 pin G2)

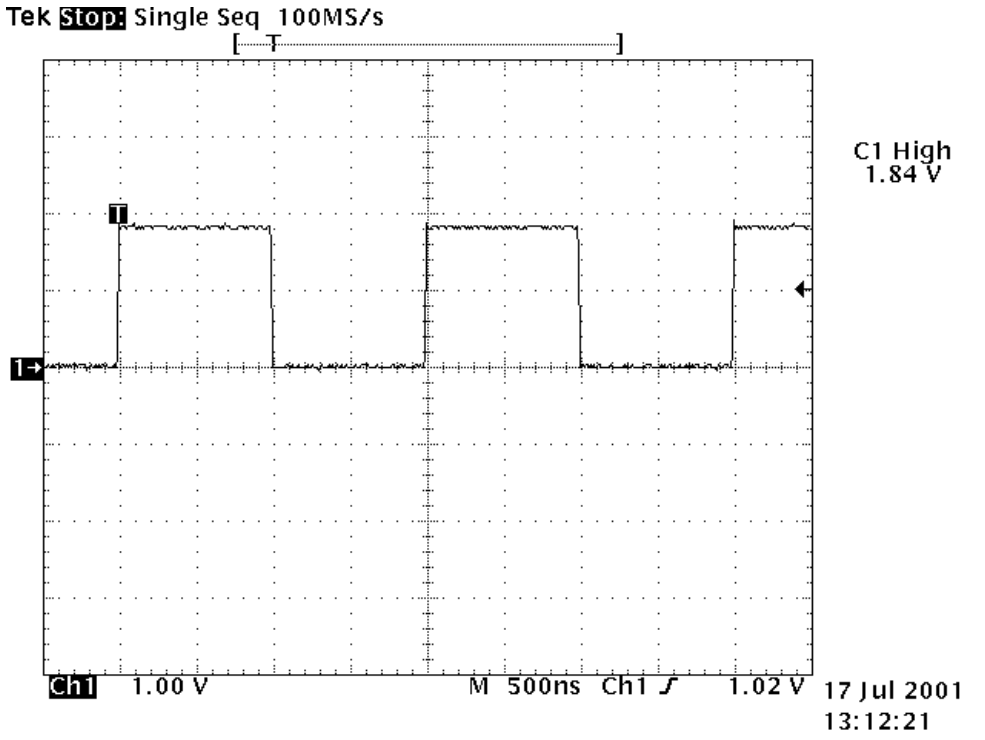


Figure 21: J408: ***CBUSENX***, UEM (D200 pin C8) -> UPP (D400 pin F3)

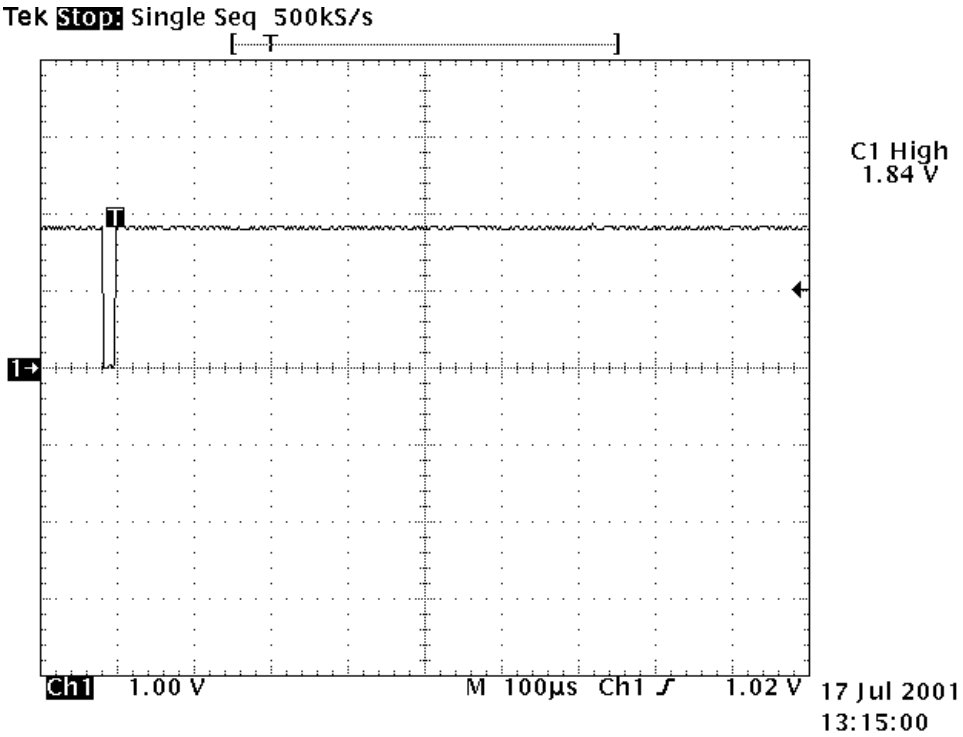


Figure 22: J409: ***MBUSTX*** (during flashing), UPP (D400 pin E3) -> UEM (D200 pin C6)

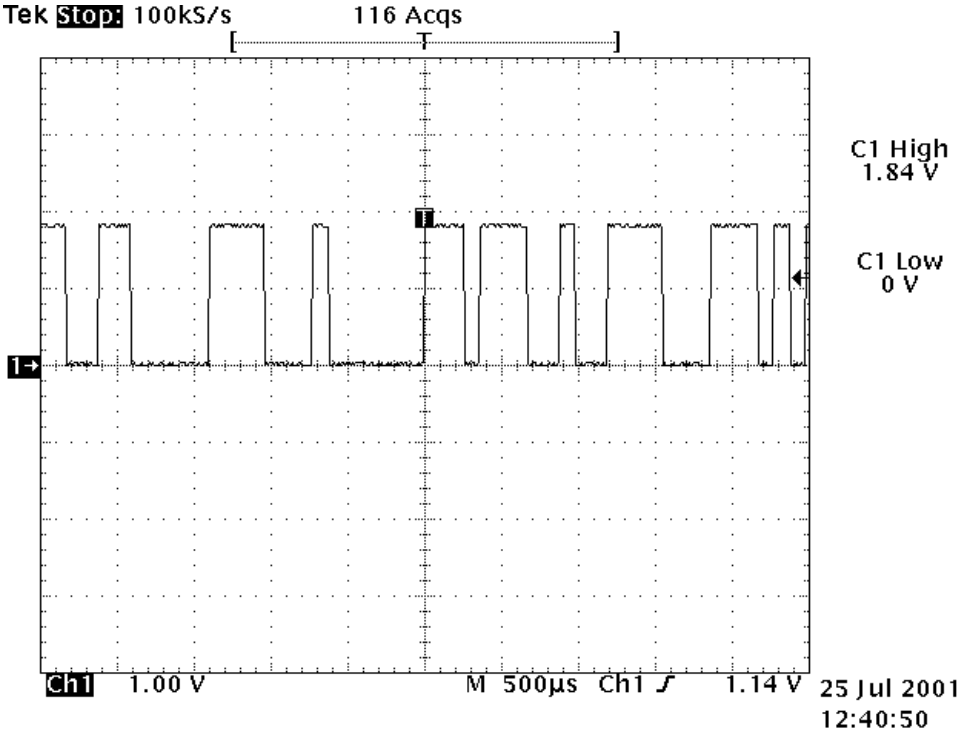


Figure 23: J410: ***MBUSRX*** (during flashing), UEM (D200 pin D6) -> UPP (D400 pin D3)

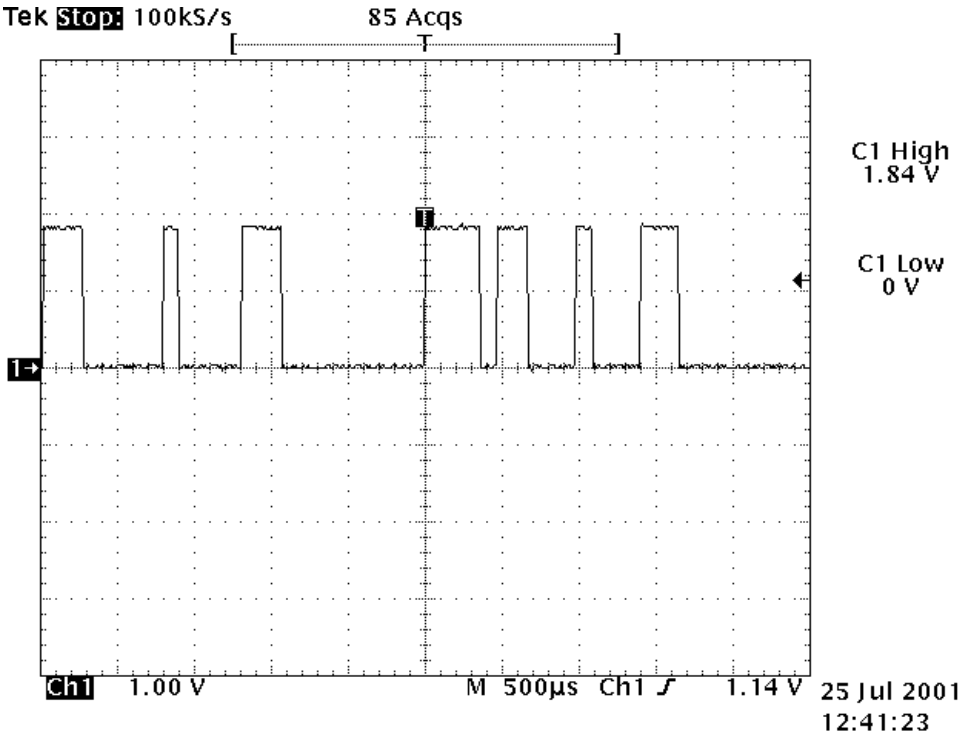


Figure 24: J411: ***FBUSTX*** (during flashing), UPP (D400 pin F1) -> UEM (D200 pin A7)

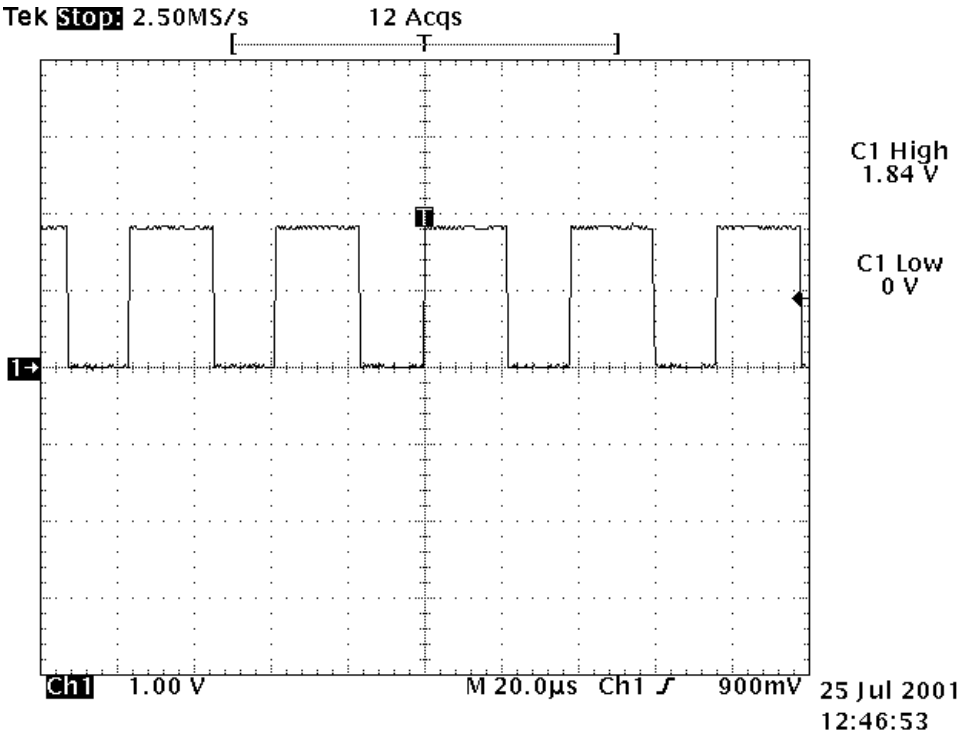


Figure 25: J412: ***FBUSRX*** (during flashing), UEM (D200 pin C7) -> UPP (D400 pin E4)

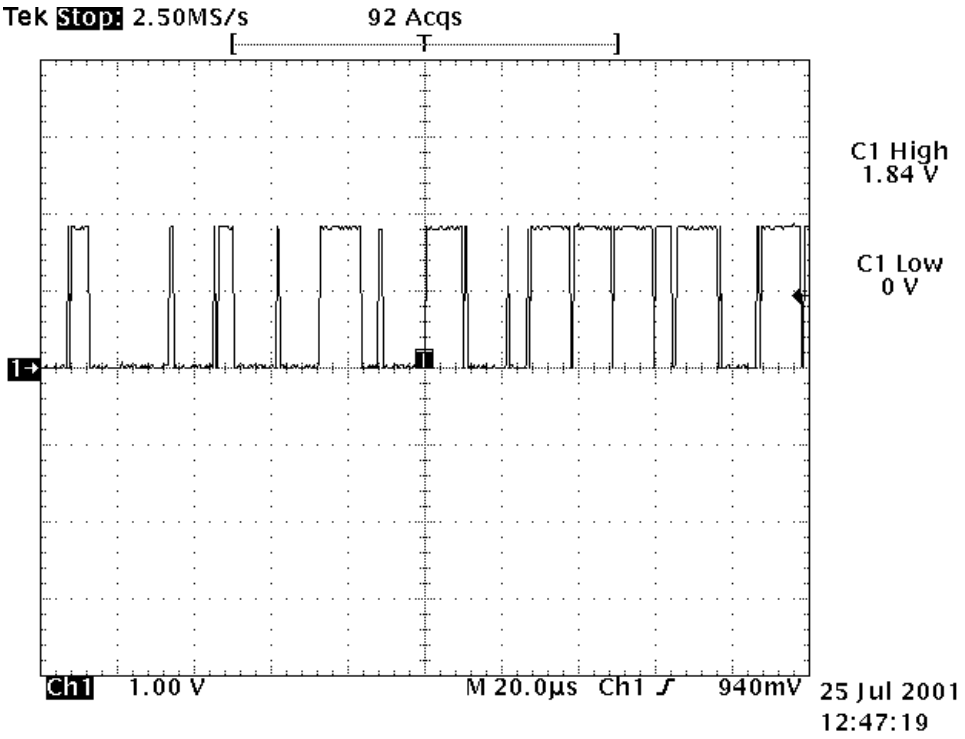


Figure 26: J413: ***DBUSCLK***, UEM (D200 pin D10) -> UPP (D400 pin K3)

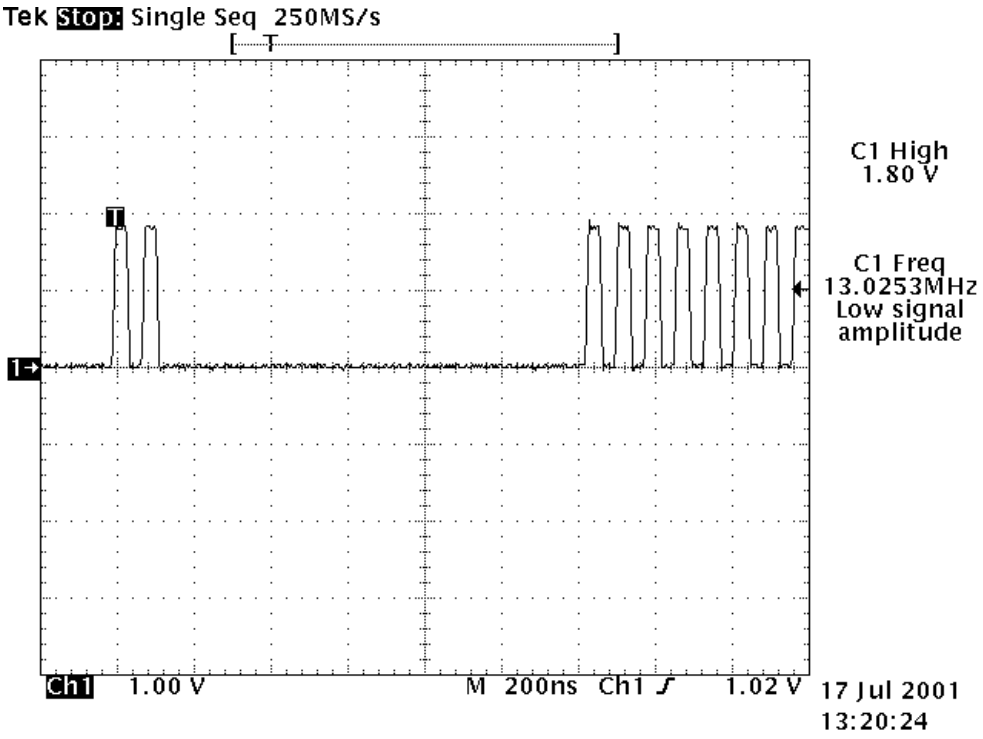


Figure 27: J414: ***DBUSDA***, UEM (D200 pin A11) <-> UPP (D400 pin L3)

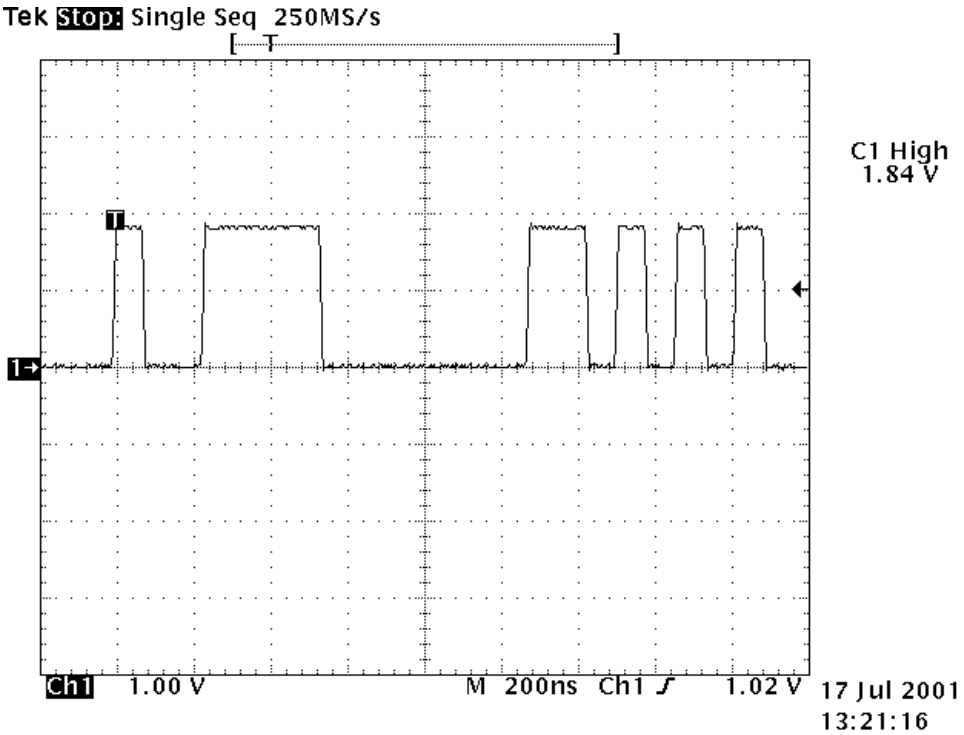


Figure 28: J415: ***DBUSENX1***, UEM (D200 pin B10) -> UPP (D400 pin J3)

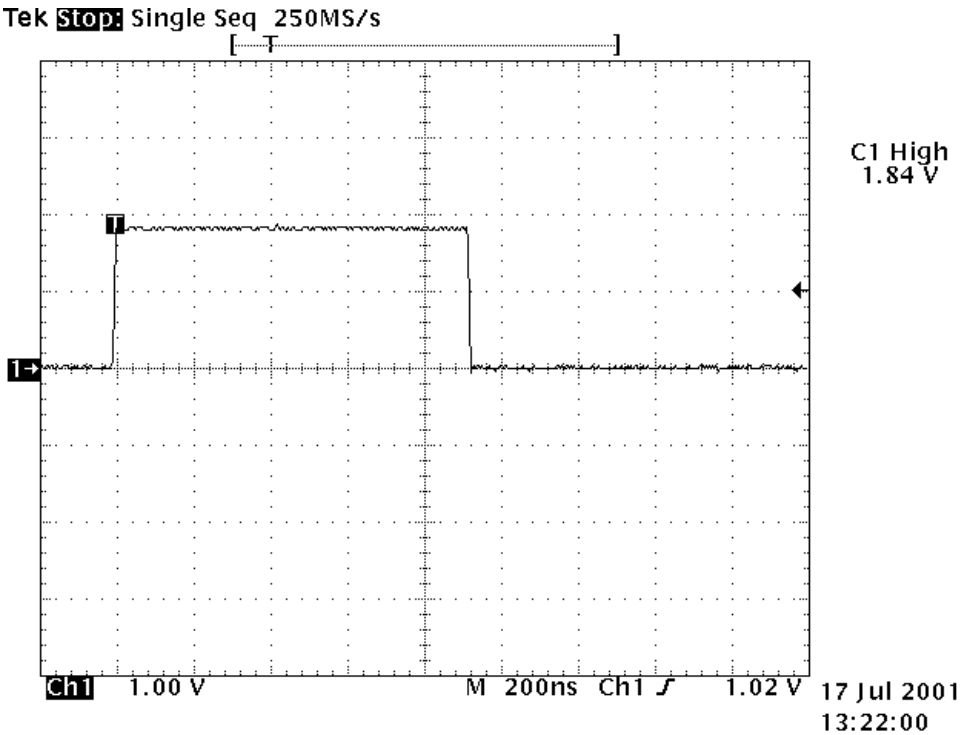


Figure 29: J416: ***EXTWRX*** (during flashing), UPP (D400 pin N9) -> FLASH (D450 pin A6)

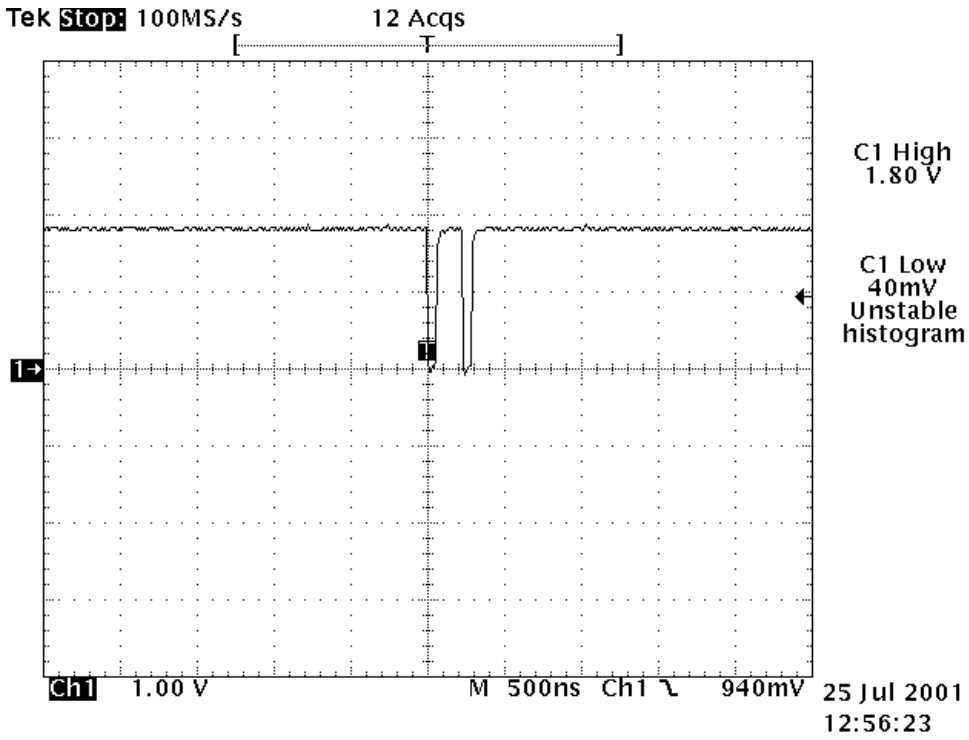


Figure 30: J417: ***EXTRDX***, UPP (D400 pin L7) -> FLASH (D450 pin C10)

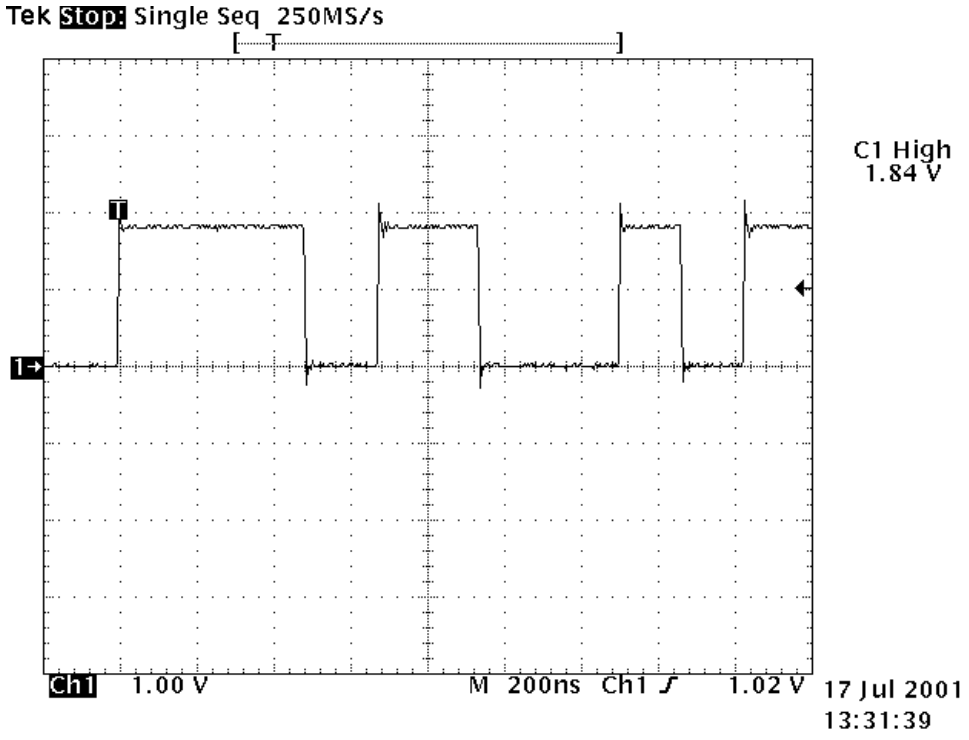


Figure 31: J419: ***FLSCLK***, UPP (D400 pin N12) -> FLASH (D450 pin A4)

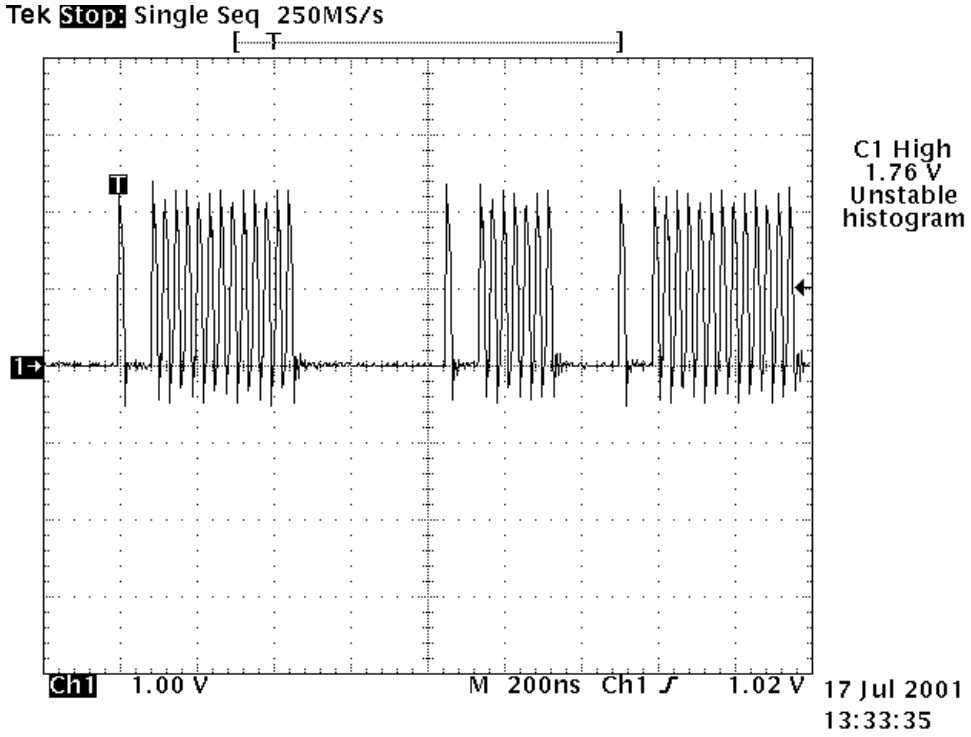


Figure 32: J420: ***FLSCSX***, UPP (D400 pin N6) -> FLASH (D450 pin B9)

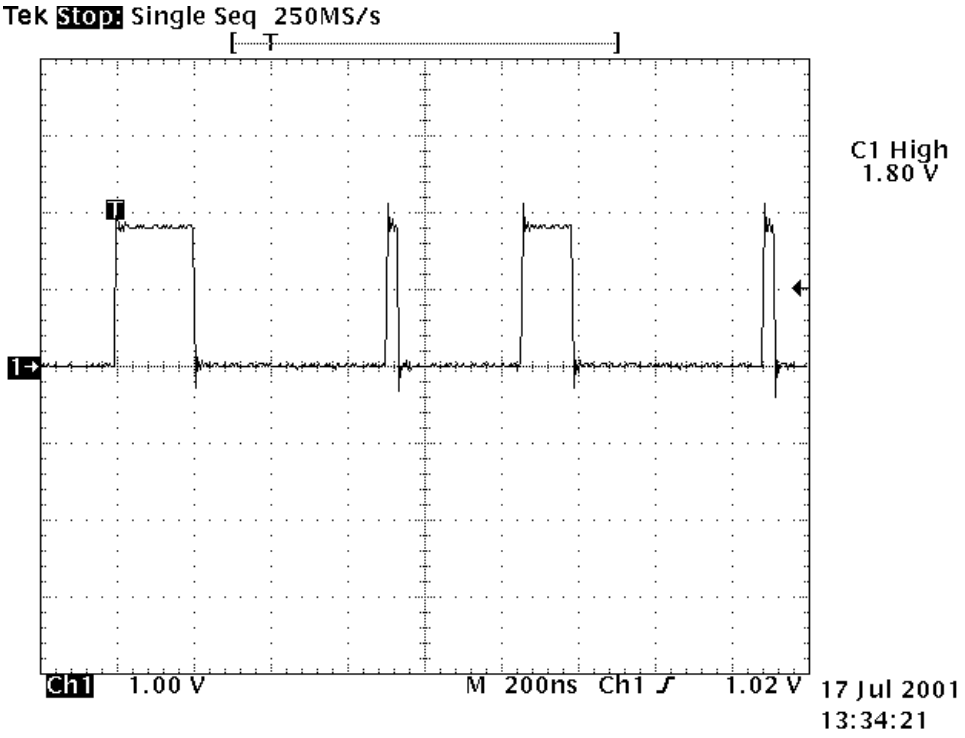


Figure 33: J700: ***TXP***, UPP (D400 pin D11) -> HAGAR (N600 pin D5)

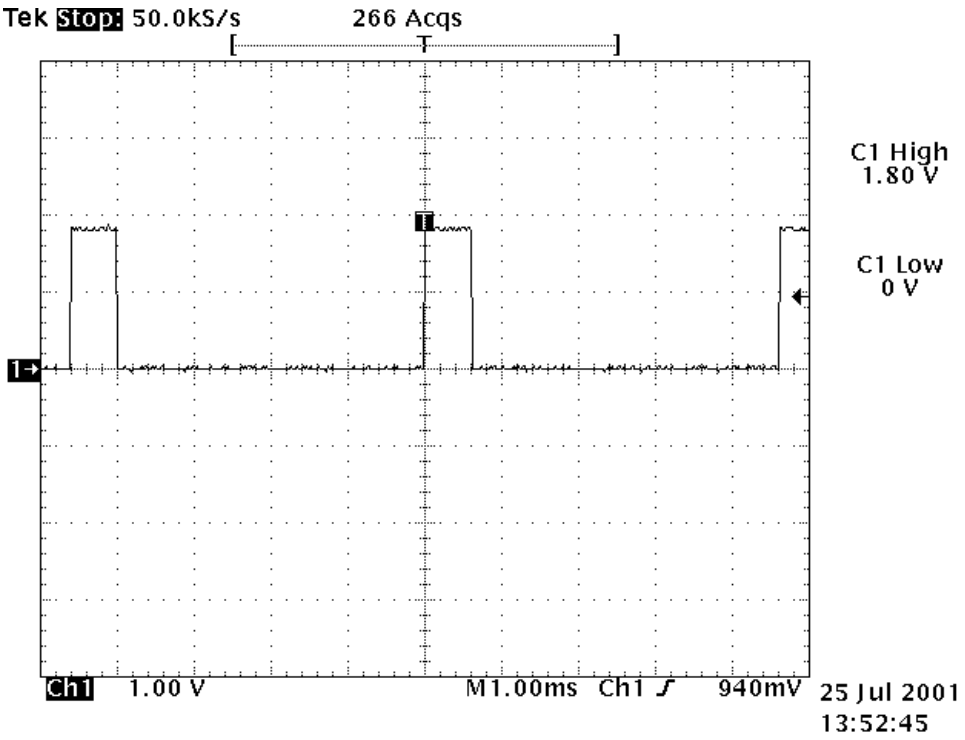


Figure 34: R301: ***PWRONX***, POWER BUTTON (S300) -> UEM (D200 pin P7)

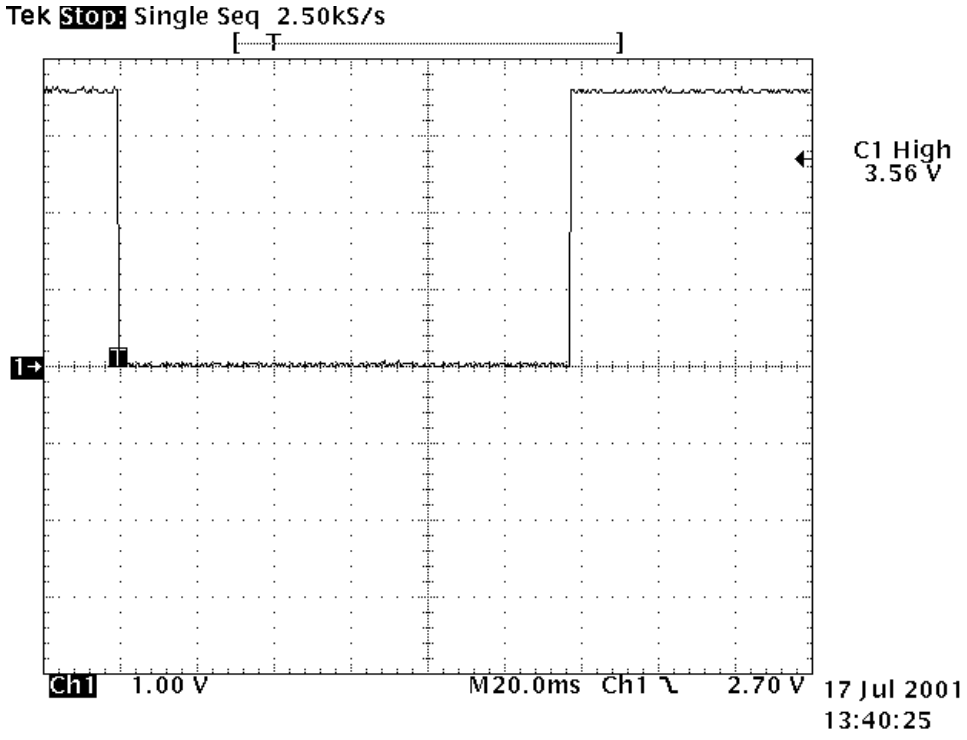


Figure 35: R305: ***KLIGHT***, UEM (D200 pin F3) -> BACKLIGHT CIRCUITRY (V300 pins 2,3,5 and V301 pins 2,5,6)

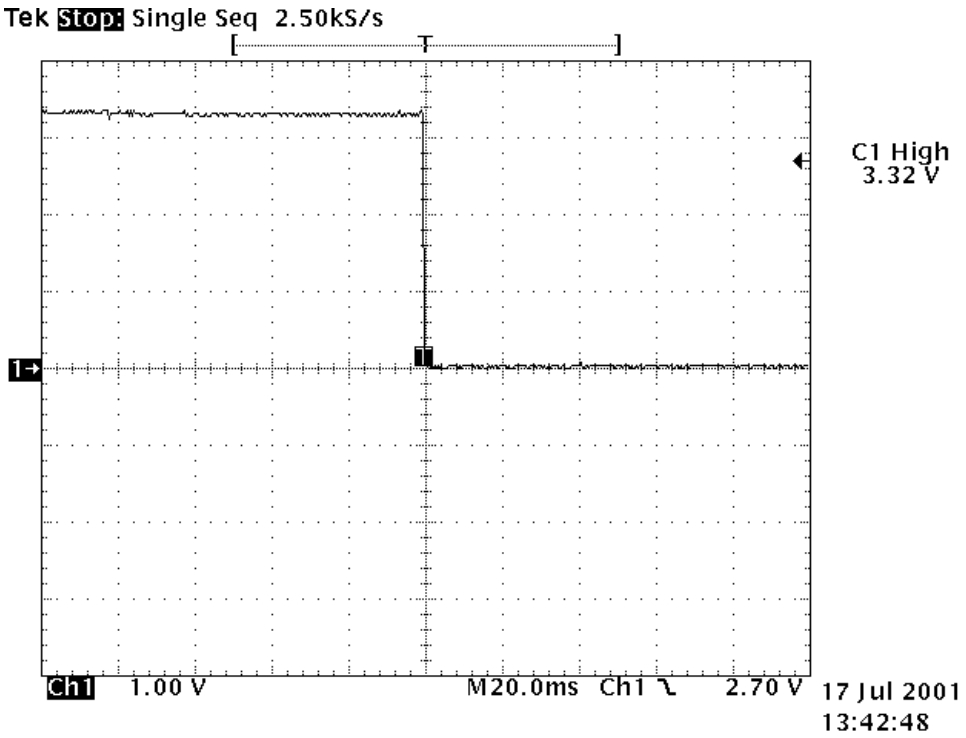


Figure 36: R420: ***RFCLK*** (13 MHz), HAGAR (N600 pin E4) -> UPP (D400 pin M5)

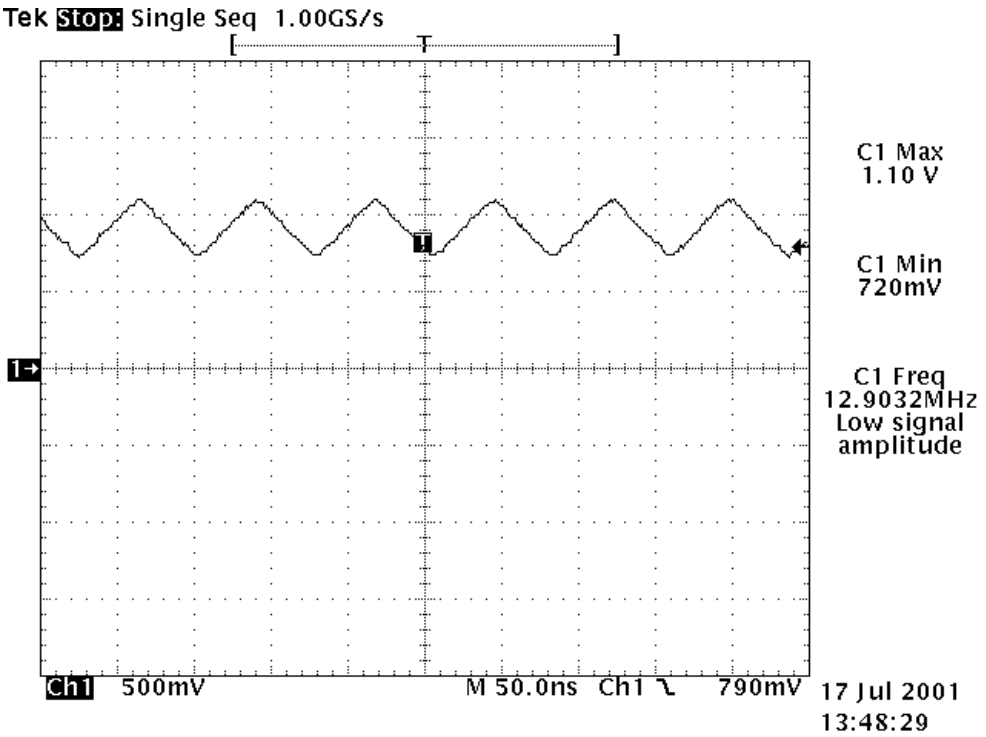


Figure 37: X100 PIN 9: ***VIBRA***, UEM (D200 pin G3) -> SYSTEM CONNECTOR (X100 pin 9)

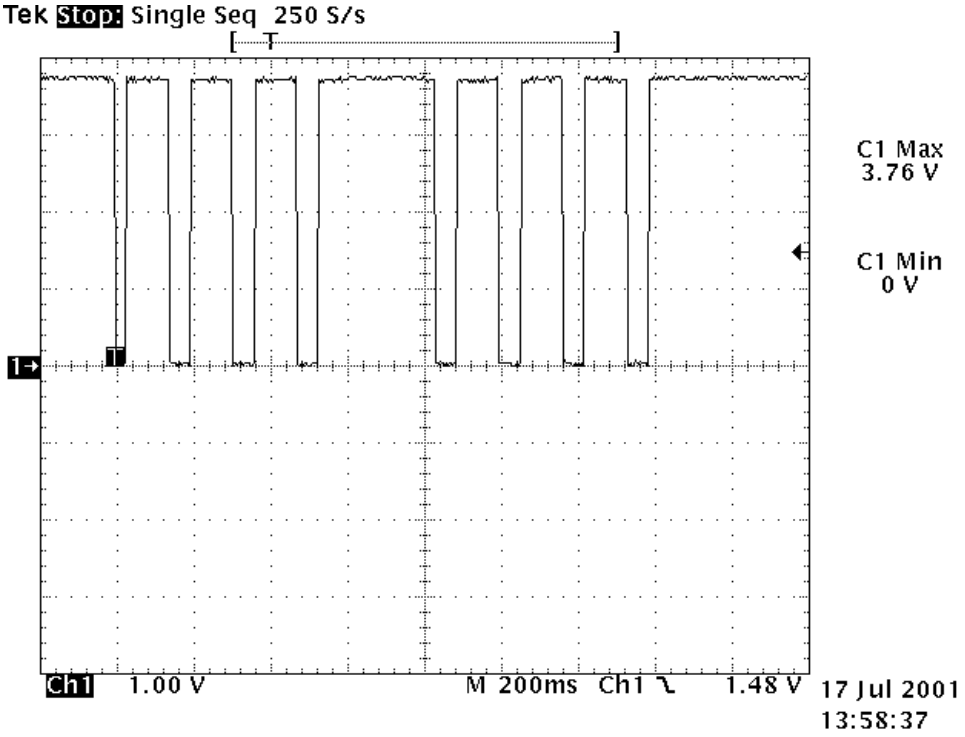


Figure 38: X300 PIN 1: ***XRES*** (startup), UPP (D400 pin A7) -> LCD CONNECTOR (X300 pin 1)

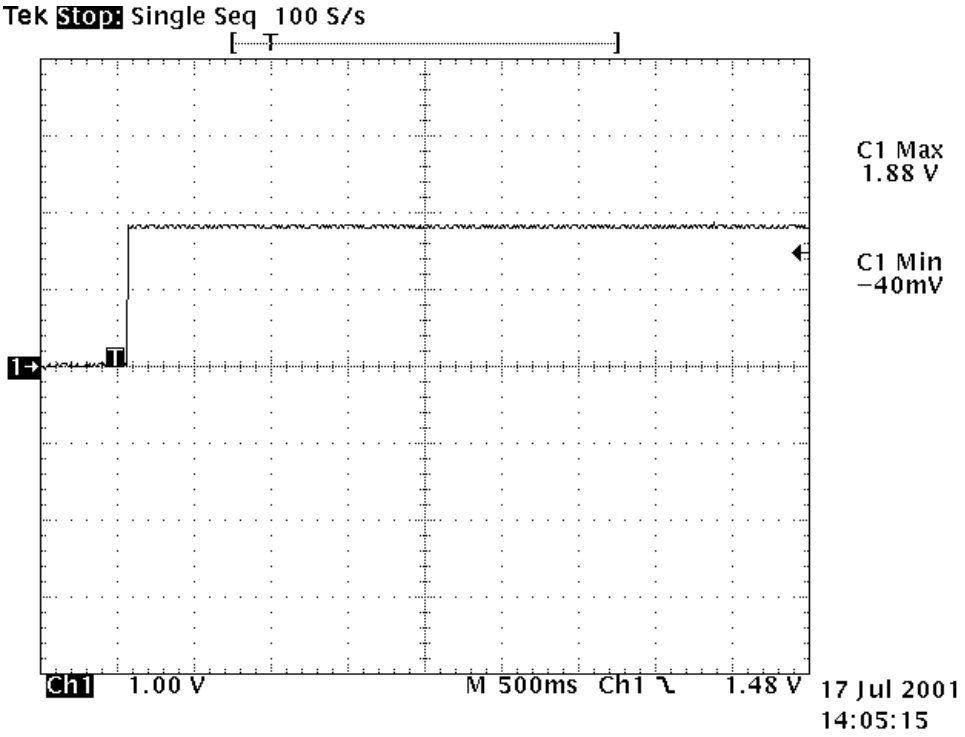


Figure 39: X300 PIN 2: ***XCS***, UPP (D400 pin C7) -> LCD CONNECTOR (X300 pin 2)

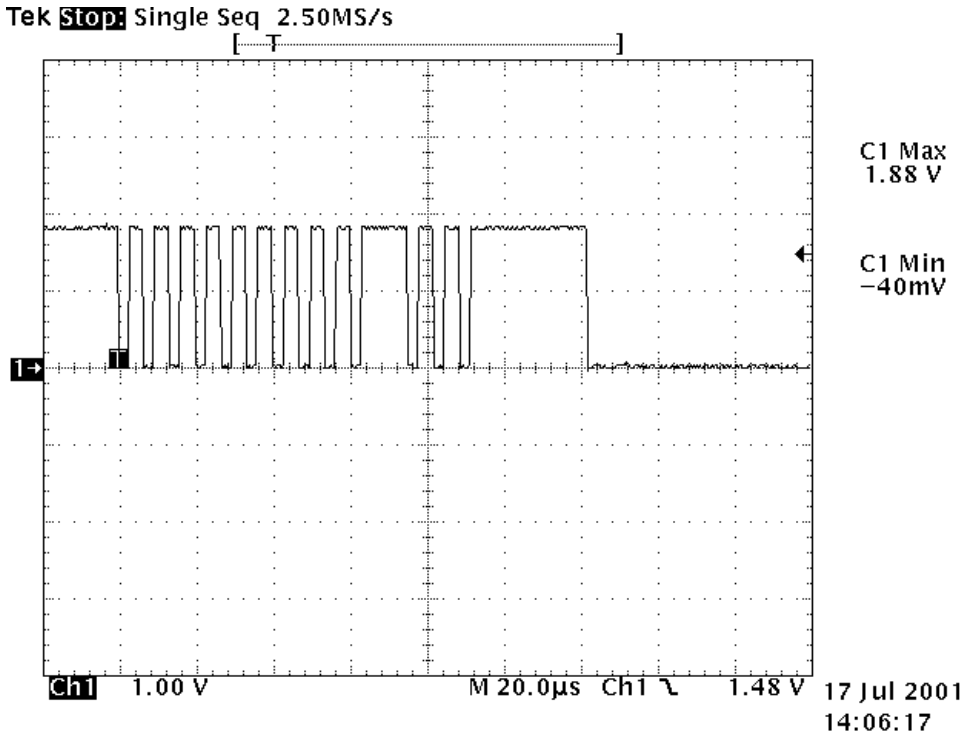


Figure 40: X300 PIN 4: ***SDA***, UPP (D400 pin B6) -> LCD CONNECTOR (X300 pin 4)

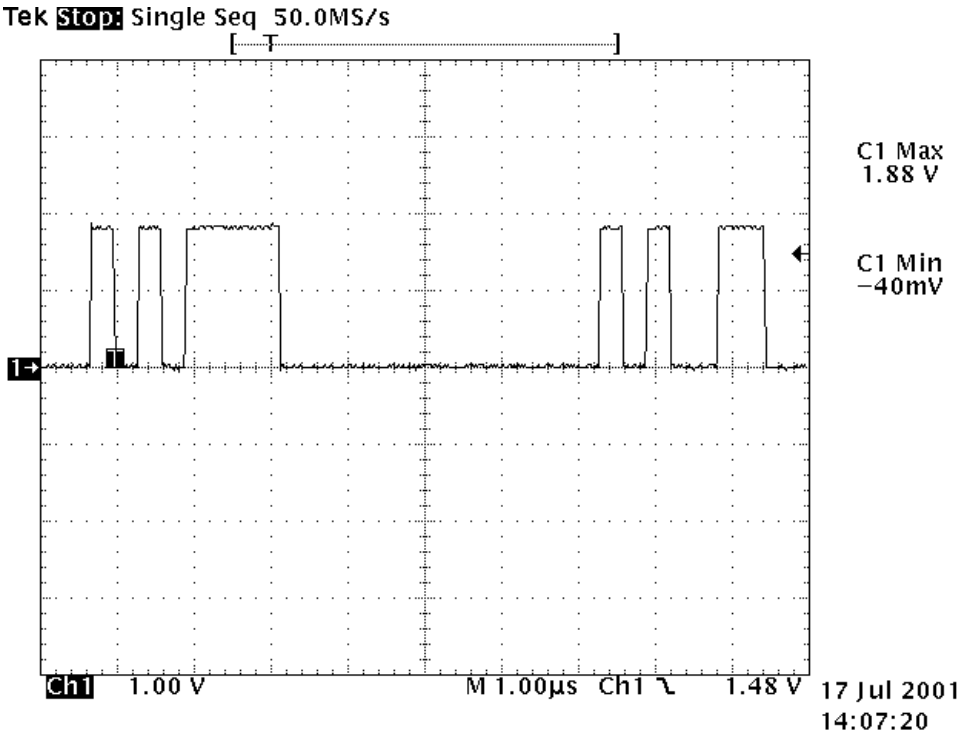


Figure 41: X300 PIN 5: ***SCLK***, UPP (D400 pin C6) -> LCD CONNECTOR (X300 pin 5)

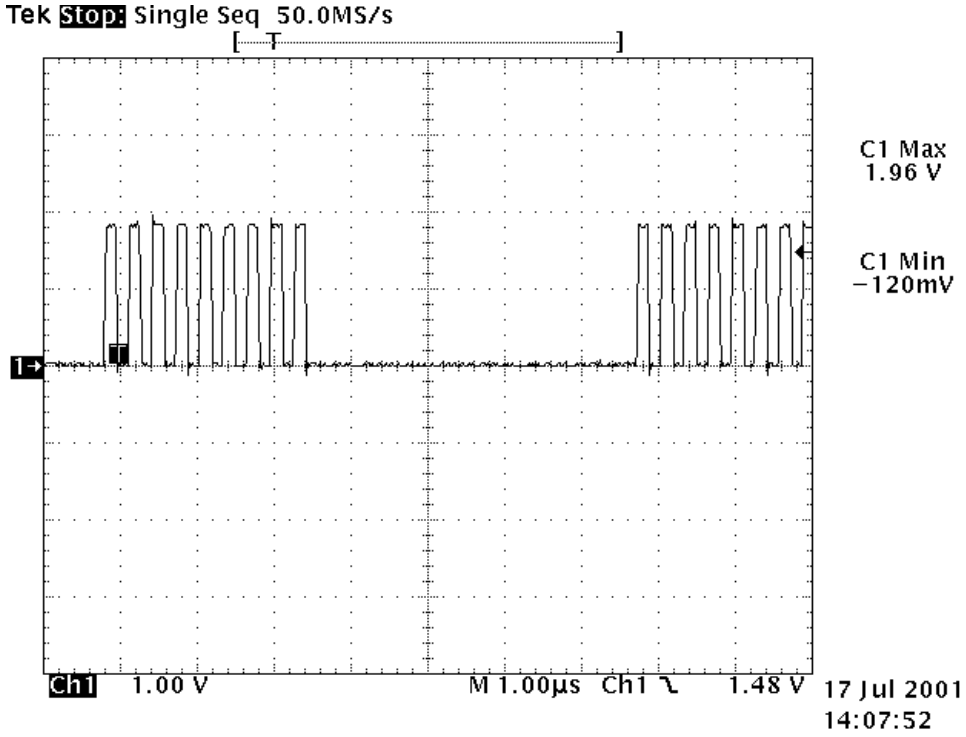


Figure 42: X300 PIN 8: ***VOUT***, LCD CONNECTOR (X300 PIN 8) -> C301 and C302

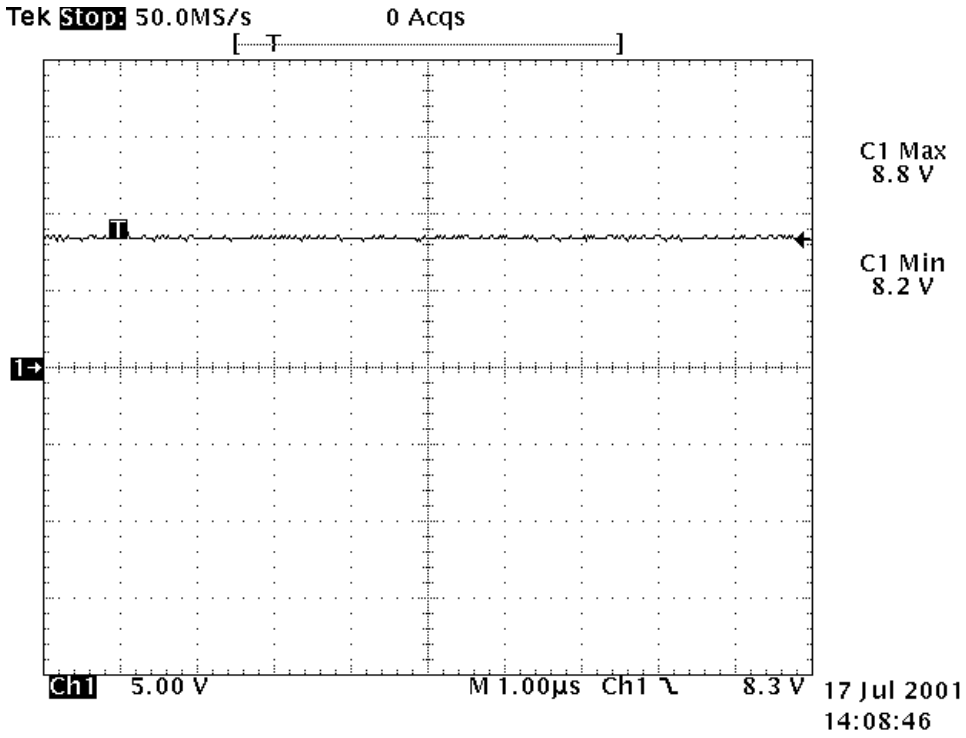
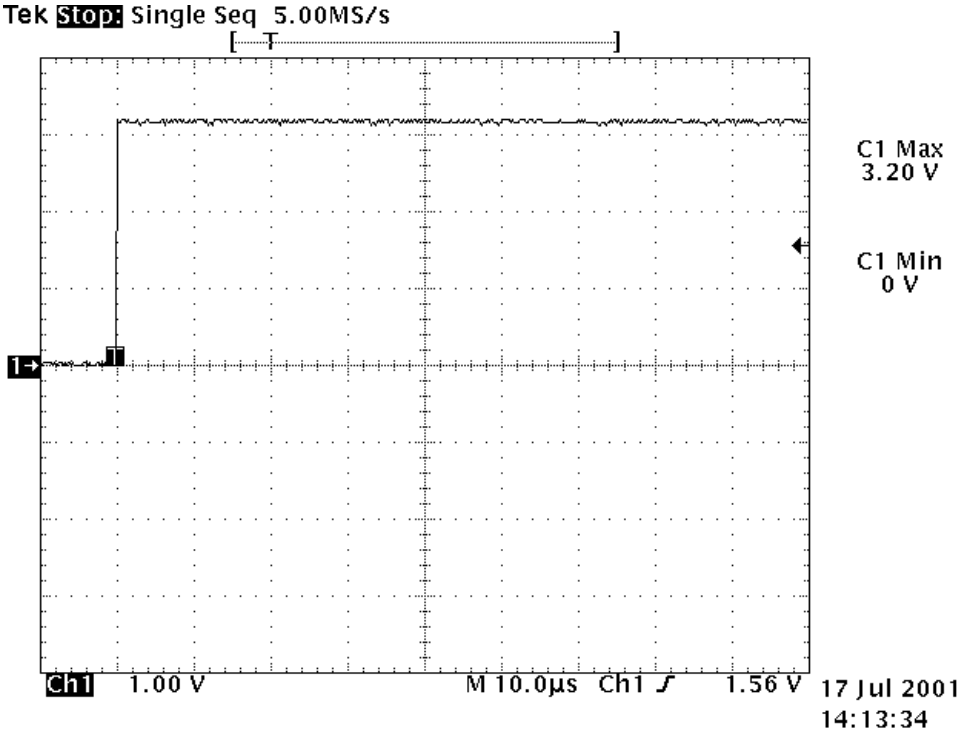


Figure 43: X303 PIN 2: ***KEYB_LIGHT***, BACKLIGHT CIRCUITRY (V300 pin 6) -> UI CONNECTOR (X303 pin 2)



Troubleshooting steps

The following hints should help to find the cause of the problem when the circuitry seems to be faulty. This troubleshooting instruction is divided into sections.

1 Phone is totally dead

2 Power does not stay on or the phone is jammed

3 Flash programming does not work

4 Display is not working

5 Plug in SIM card is out of order (insert SIM card).

6 Audio fault

7 Charging fault

The first thing to do is carry out a through visual check of the module. Ensure in particular that:

a) there are no mechanical damages

b) soldered joints are OK.

General instructions

Most semiconductors are static discharge sensitive! ESD protection must be taken care of during repair (ground straps and ESD soldering irons). HAGAR, PA, UEM, UPP, and Flash are moisture sensitive and must be pre-baked prior to soldering, if they have been out of their vacuum package longer than the specified time.

- Connect test jig to computer with DAU-9S cable or to FPS-8 Flash Prommer with AXS-4 serial cable.
- Make sure that you have PKD-1 dongle connected to computer's parallel port.
- Connect DC power supply to module test jig with FLC-2 cable.
- Set the DC supply voltage to 3.9 V and set the module test jig (MJS-46) jumper connector to "bypass" position. VBAT must not exceed 5.15 V to avoid damaging the power amplifier (PA), if PA is active.
  - MJS-46's current consumption is ~ 9 mA. Note that MJS-46 is not protected against reverse voltage and there is a 2 A fuse which may blow if the phone is short-circuited.
- When doing BB energy management (EM) calibrations use JBV-1 jig and DC supply voltage 12 – 15 V.
  - JBV-1's current consumption is ~ 40 mA with 3.9 V supply voltage and ~ 80 mA with 15 V supply voltage.
- Set the phone module to test jig and start Phoenix service software. Initialize connection to phone (use FBUS driver when using DAU-9S and COMBOX driver when using FPS-8).

Note! If a "No power" problem is found, please check the A-cover fit. For more information see section Assembly & Disassembly Instructions of NSM-9DX Service Manual, page 9.

PROGRAMMING FLASH

Fails in Programming Flash -Start:

- Most probably the phone has not started up properly for flashing.
- Try flashing with Phoenix (Figure 46).
- If flashing with Phoenix is not OK, check error code from the Phoenix window (Figure 47) and check (Table 2: Flash Programming error codes) for what is not working properly.

Figure 44: Flashing with Phoenix.

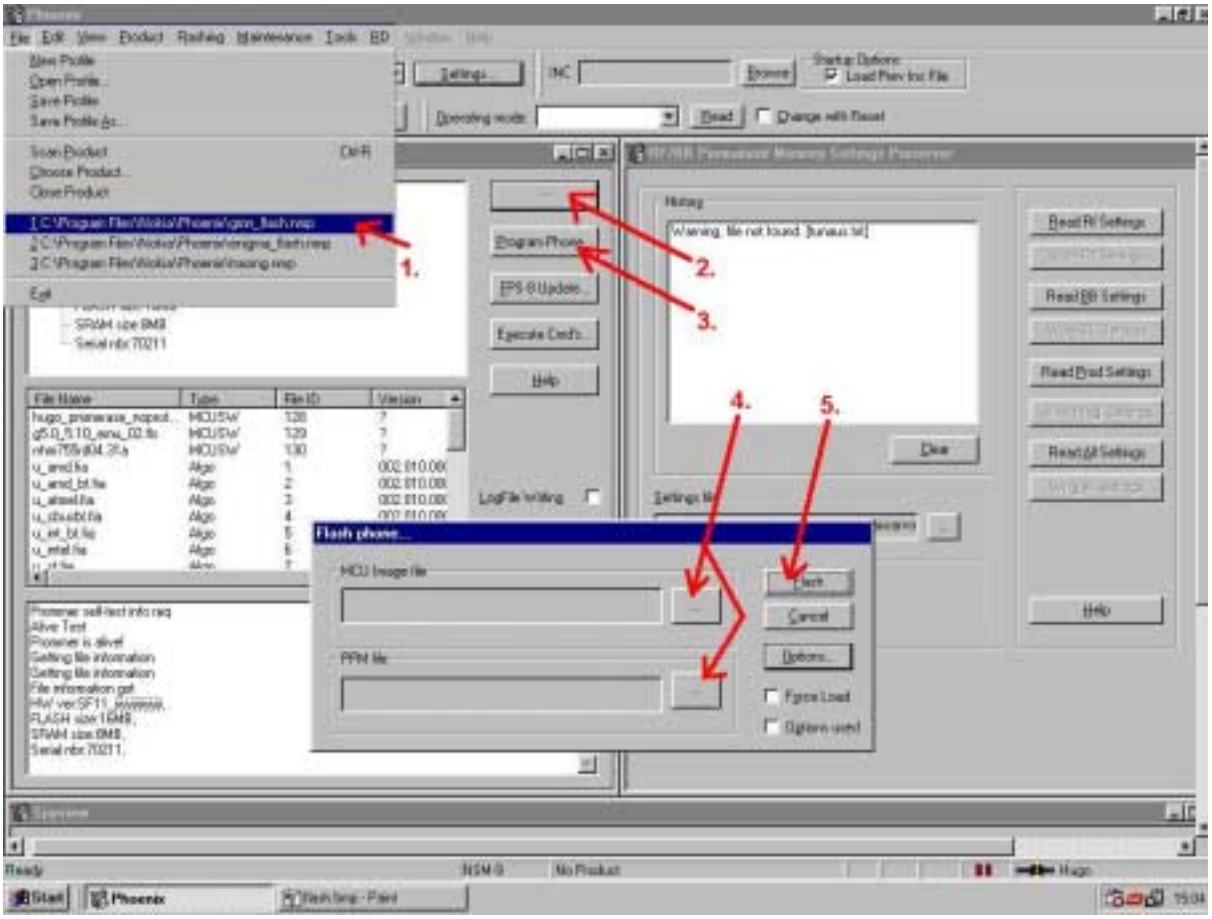


Figure 45: Error code in "Prommer Tool" window.

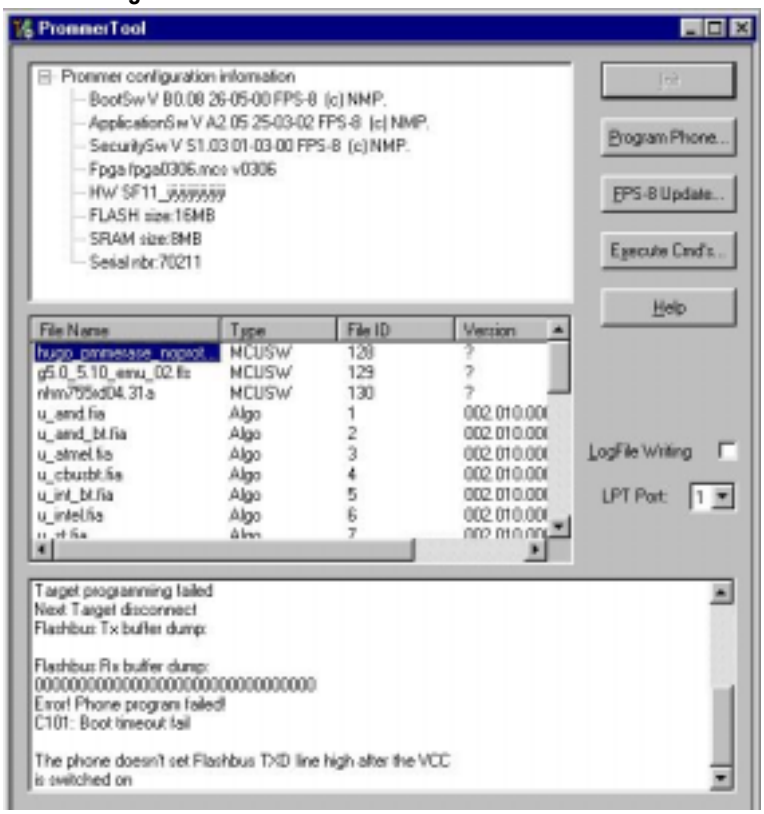


Table 2: Flash programming error codes.

Error	Description	Not working properly
C101	“Boot timeout fail” "The phone does not set Flashbus TXD line high after the VCC is switched on."	**Vbatt** **Vflash1** **Vcore** **VIO** **BSI and FbusRX from prommer to UEM.** **FbusTx from UPP -> UEM -> prommer (SA0)**
C102	"The phone doesn’t set Flashbus TXD line low after the line has been high. This error is received also when the phone is not connected to the prommer."	**PURX (also to Hagar)** **VR3** **RFCLK (VCTCXO -> Hagar -> UPP)** **Mbus from prommer -> UEM -> UPP (MbusRx) (SA1)** **FbusTx from UPP -> UEM -> prommer (SA1)**
C103	"Boot serial line fail." “The phone MCU hasn’t received the first dummy word correctly from the prommer after the phone VCC is switched on.”	**Mbus from prommer -> UEM -> UPP (MbusRx) (SA0)** **FbusRx from prommer -> UEM -> UPP** **FbusTx from UPP -> UEM -> prommer**
C104	"MCU ID message sending failed in the Phone."	**FbusTx from UPP -> UEM -> prommer**
C105	"The phone has not received Secondary boot codes length bytes correctly."	**Mbus from prommer -> UEM -> UPP (MbusRx)** **FbusRx from prommer -> UEM -> UPP** **FbusTx from UPP -> UEM -> prommer**
C106	"The phone has not received Secondary code bytes correctly."	**Mbus from prommer -> UEM -> UPP (MbusRx)** **FbusRx from prommer -> UEM -> UPP** **FbusTx from UPP -> UEM -> prommer**
C107	"The phone MCU can not start Secondary code correctly."	**UPP**
A187	“Wrong MCU ID” "The MCU ID in the FIASCO_MCU_ID_INFO block of the secondary boot file doesn’t match with the ID received from the target phone.”	**UPP**
A204	" The flash manufacturer and device IDs in the existing Algorithm files do not match with the IDs received from the target phone."	**Flash** **Signals between UPP and Flash**
A387	“Wrong MCU ID” "The MCU ID in the FIASCO_MCU_ID_INFO block of the MCUSW file doesn’t match with the ID received from the target phone.”	**UPP**

C601	"The prommer has detected that VPP voltage level has dropped below the limit"	**VPP from prommer -> Flash**
C383 C583 C683	"The prommer has not received phone acknowledge to the message." (C383-during algorithm download to target phone) (C583-during erasing) (C683-during programming)	**Flash** **UPP** **Signals between UPP and Flash**
C384 C584 C684	"The phone has generated NAK signal during data block transfer." (C384-during algorithm download to target phone) (C584-during erasing) (C684-during programming)	**Flash** **UPP** **Signals between UPP and Flash**
C585 C685	Data block handling timeout" (C585-during erasing) (C685-during programming)	**Flash** **UPP** **Signals between UPP and Flash**
C586 C686	"The status response from the phone informs about fail." (C586-during erasing) (C686-during programming)	**Flash**

Figure 46: Top

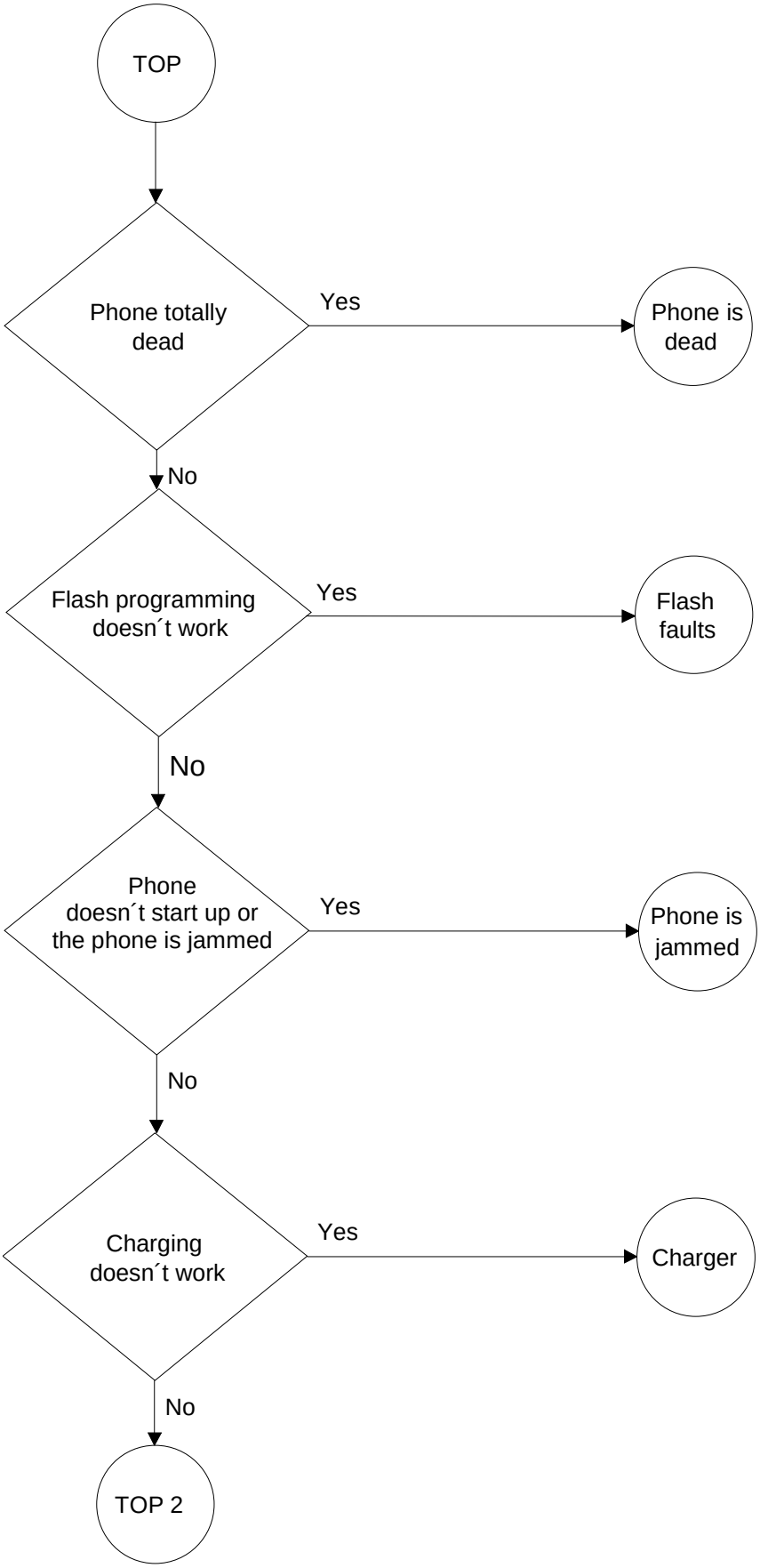


Figure 47: Top2

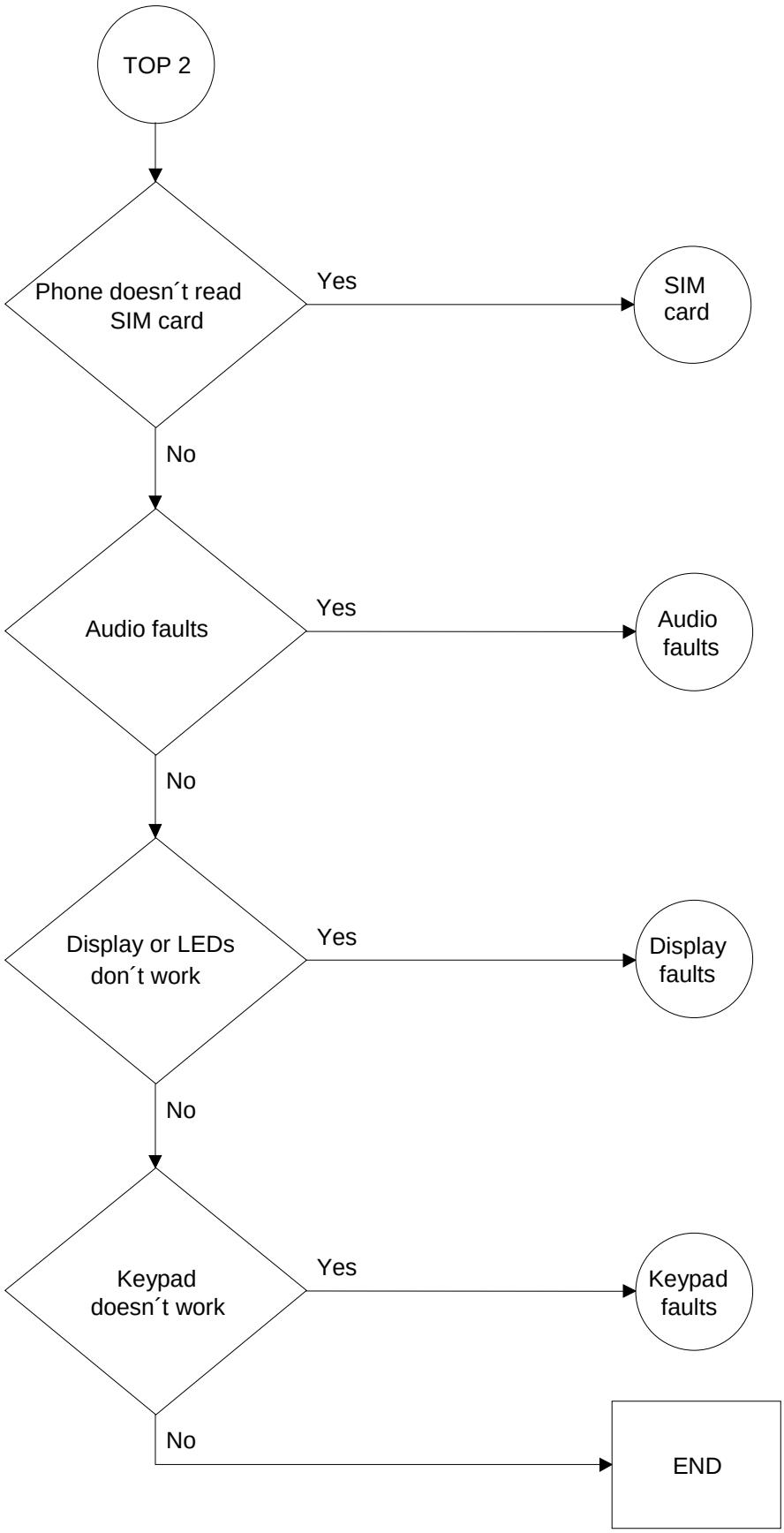


Figure 48: Phone is dead

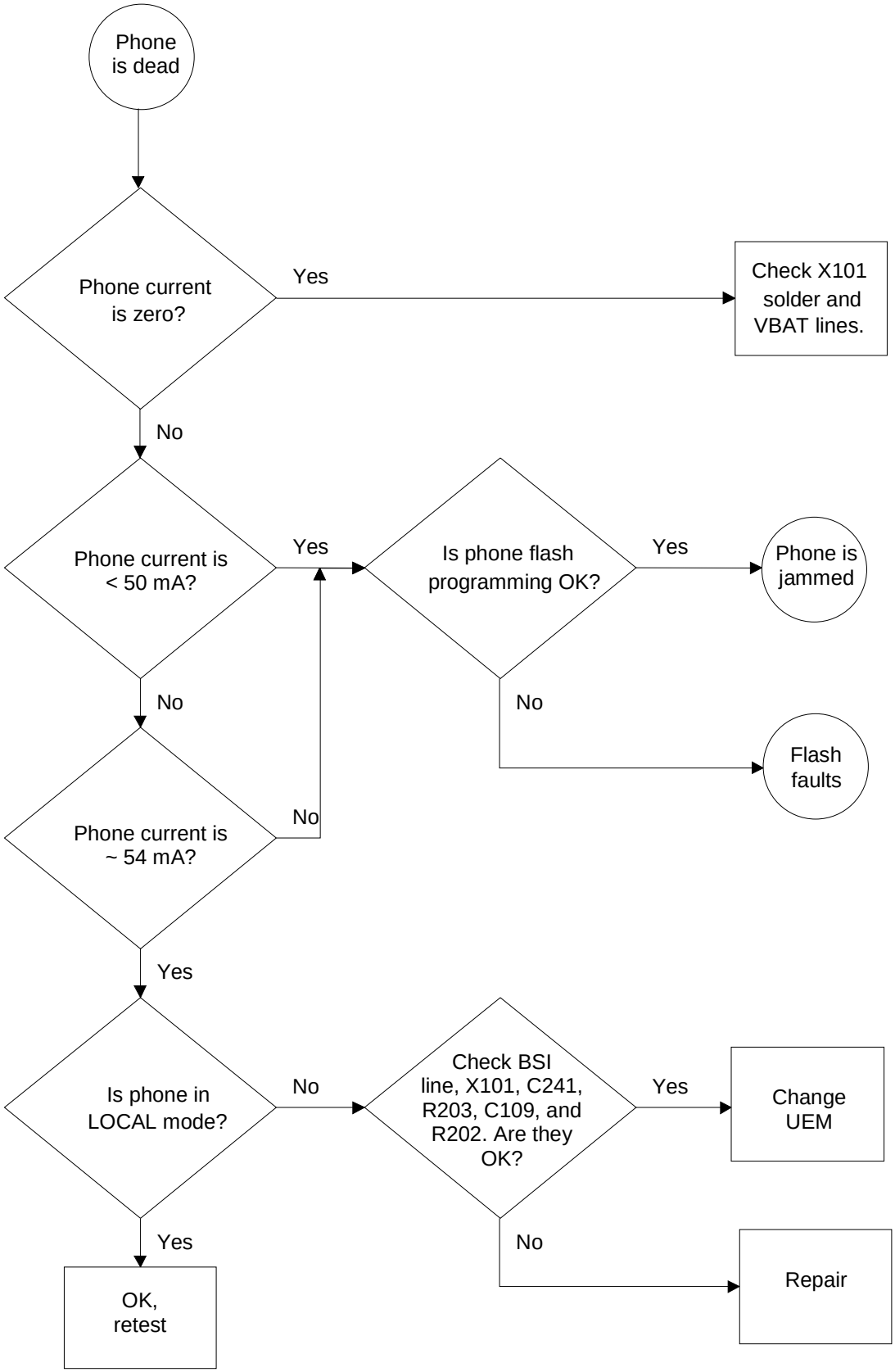
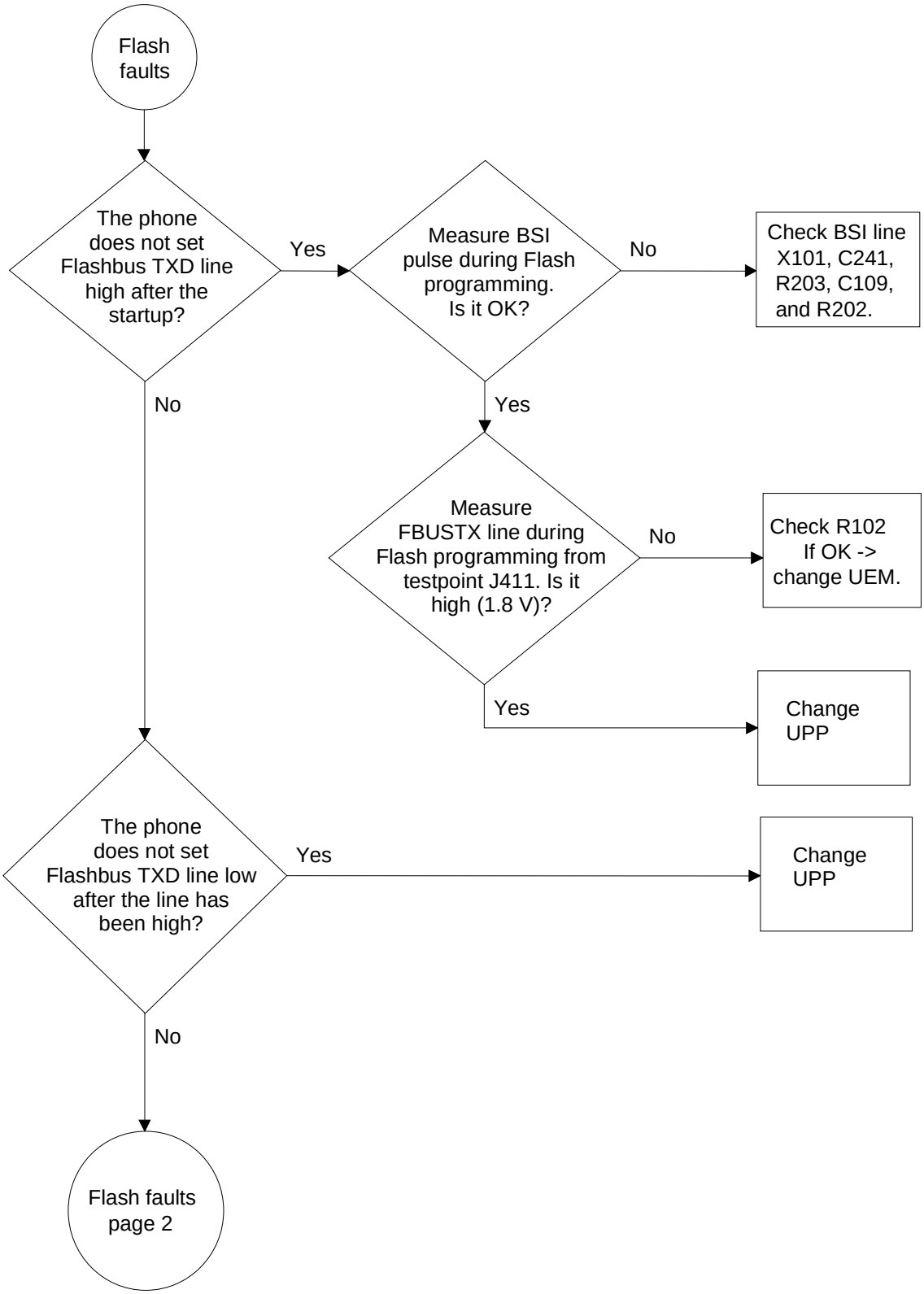


Figure 49: Flash Faults



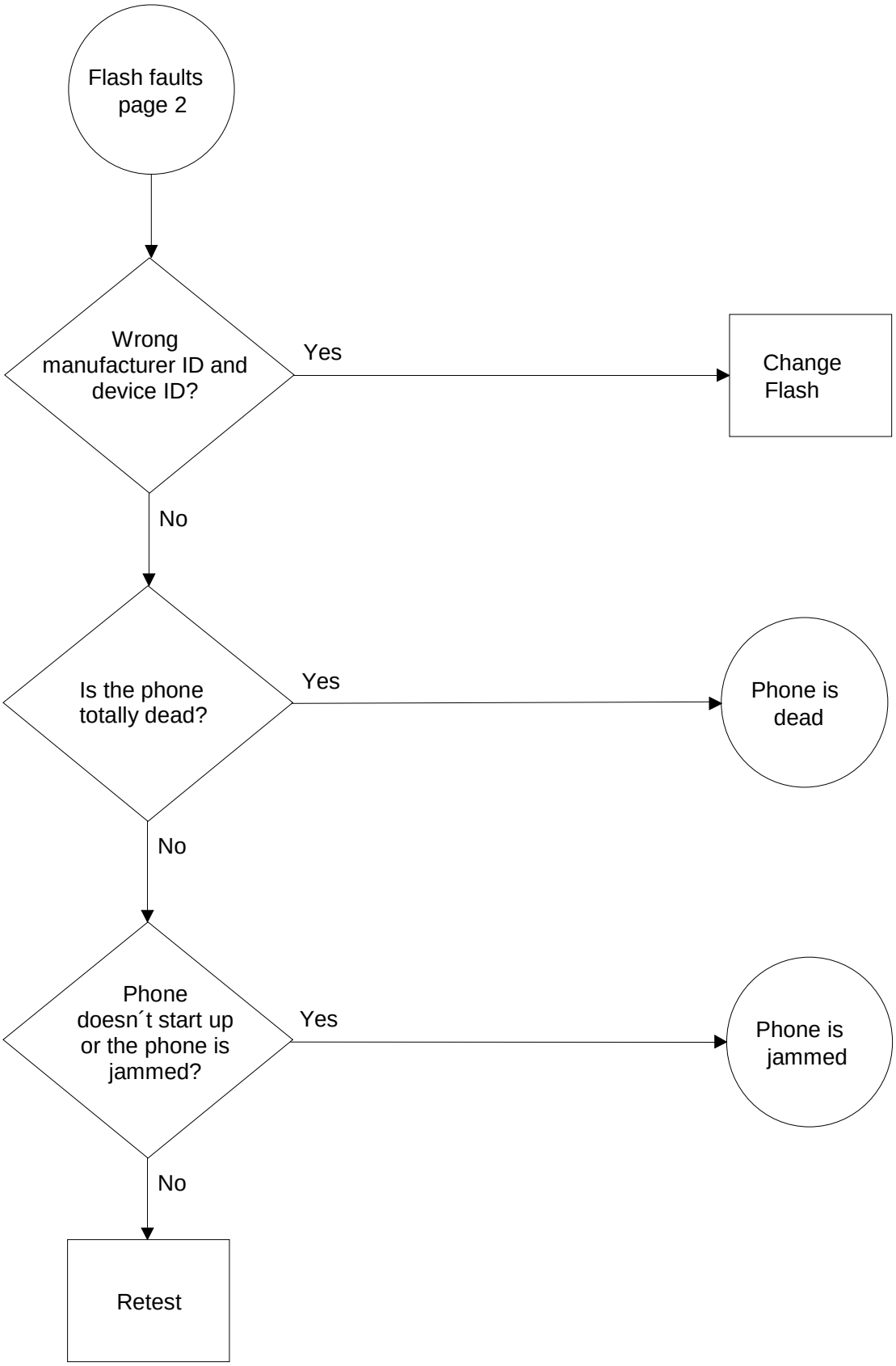
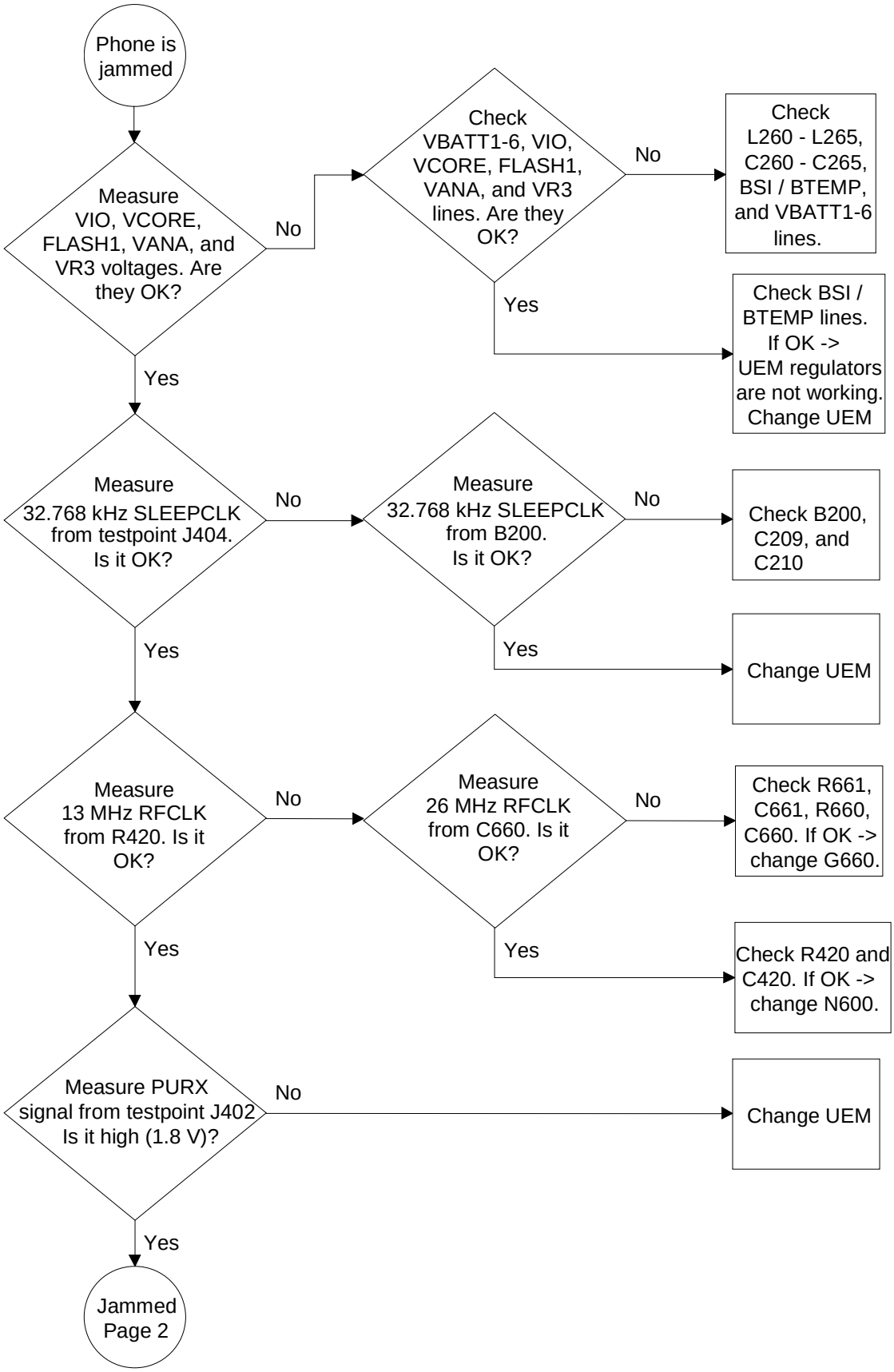

Flash faults page 2
Wrong manufacturer ID and device ID?
Yes
Change Flash
No
Is the phone totally dead?
Yes
Phone is dead
No
Phone doesn´t start up or the phone is jammed?
Yes
Phone is jammed
No
Retest

Figure 50: Phone is jammed



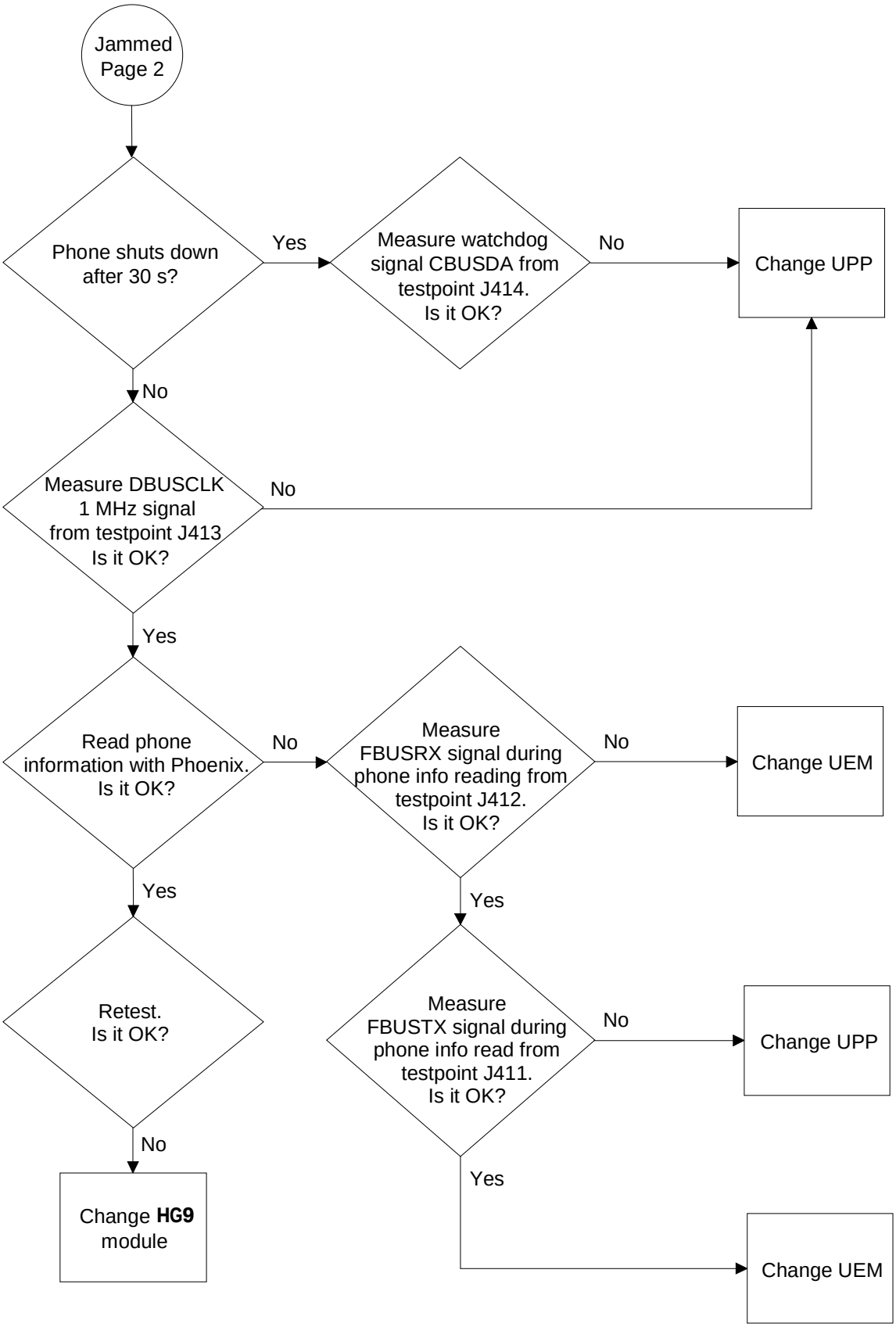

Jammed
Page 2
Phone shuts down after 30 s?
Yes
Measure watchdog signal CBUSDA from testpoint J414. Is it OK?
No
Change UPP
No
Measure DBUSCLK 1 MHz signal from testpoint J413 Is it OK?
No
Yes
Read phone information with Phoenix. Is it OK?
No
Measure FBUSRX signal during phone info reading from testpoint J412. Is it OK?
No
Change UEM
Yes
Yes
Retest. Is it OK?
Measure FBUSTX signal during phone info read from testpoint J411. Is it OK?
No
Change UPP
No
Yes
Change HG9 module
Change UEM

Figure 51: Charging Faults

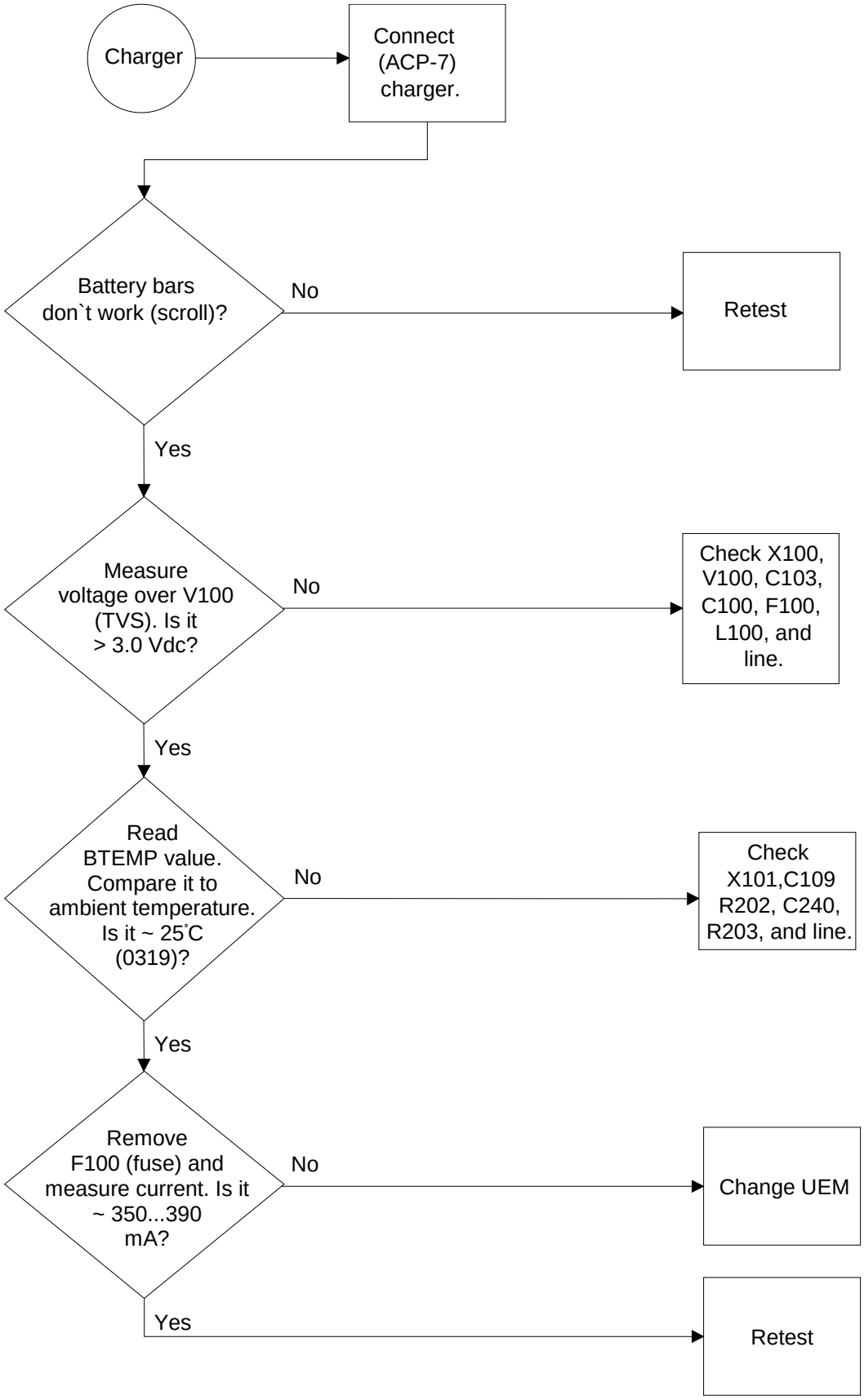


Figure 52: SIM Card

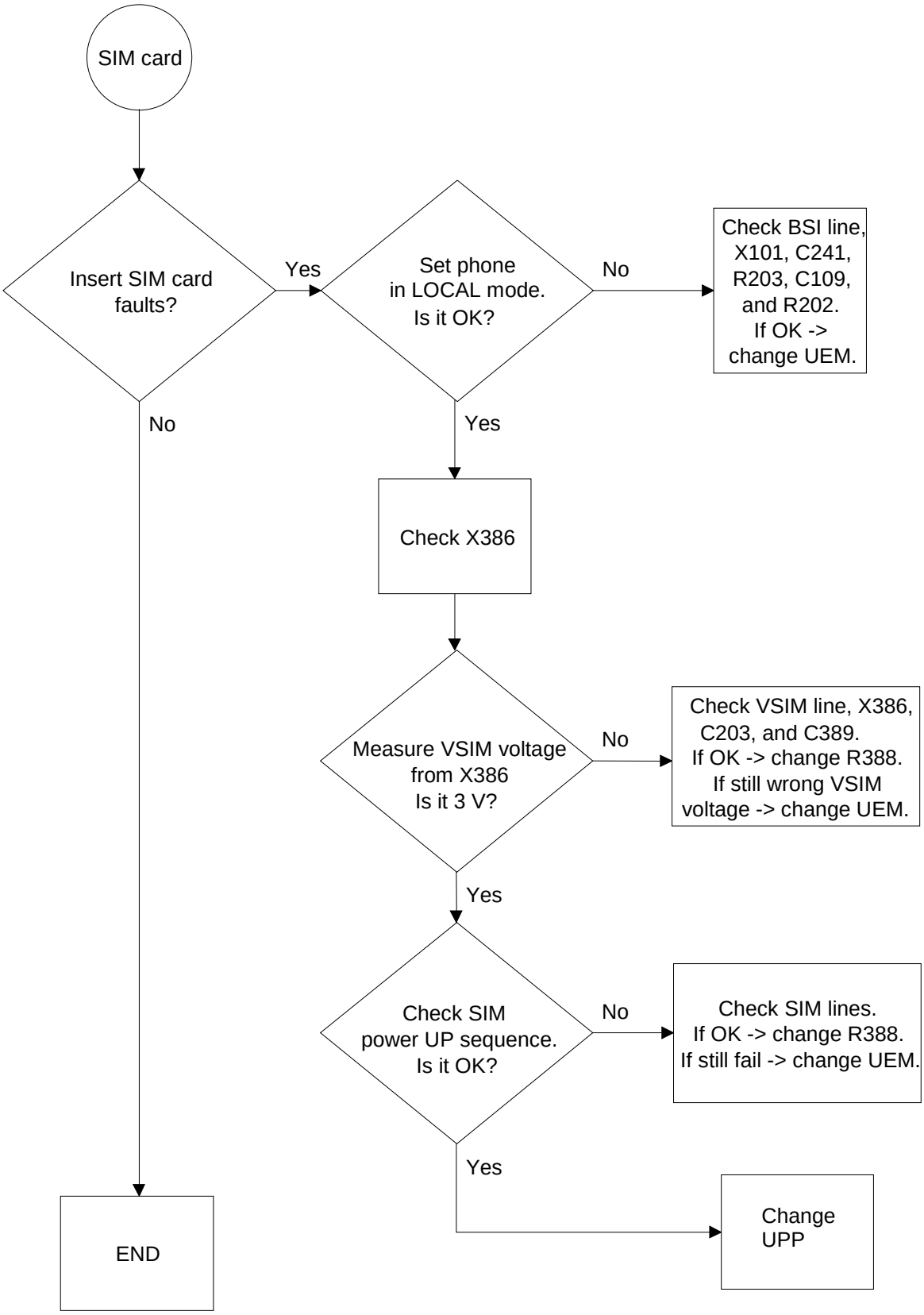
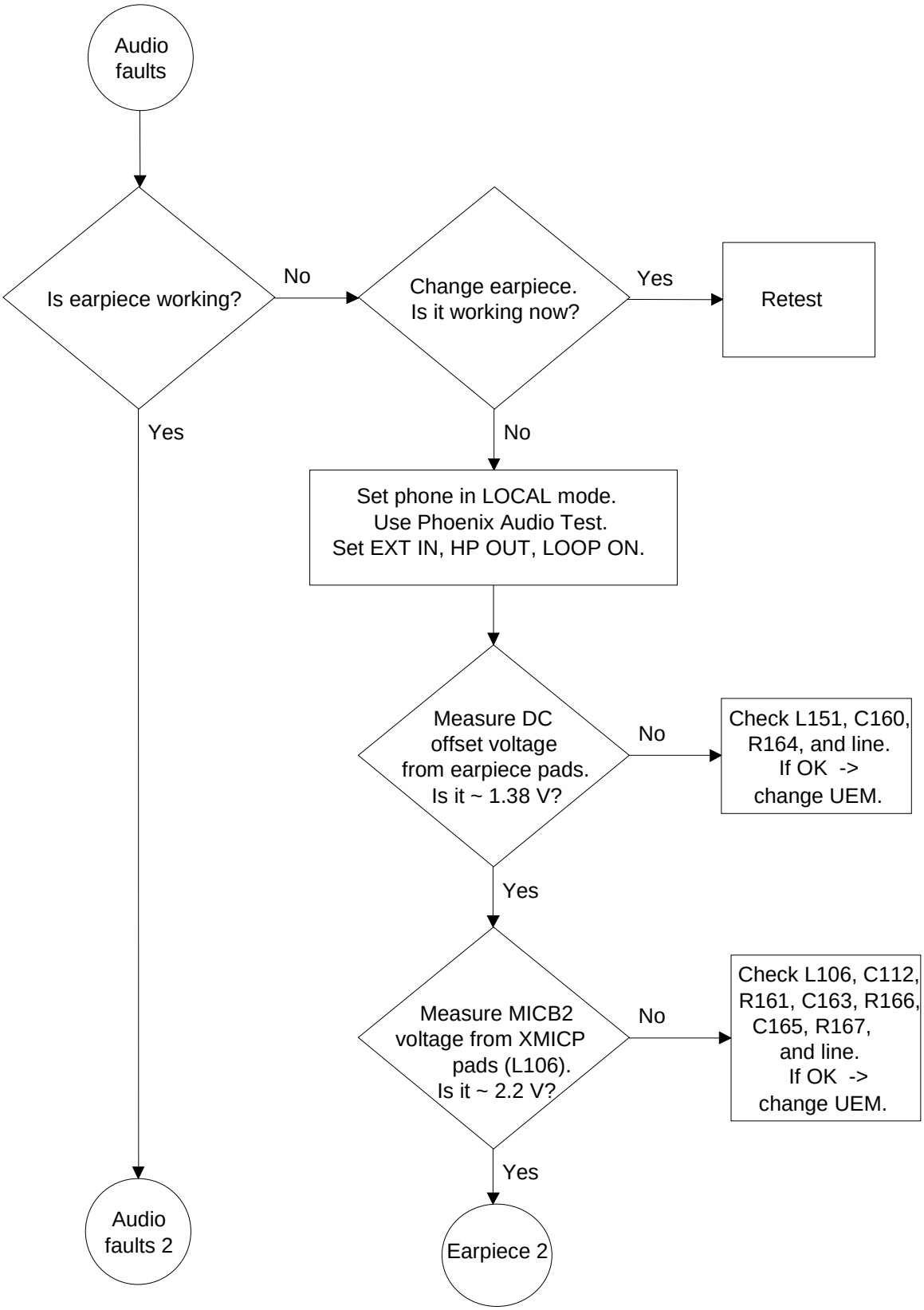
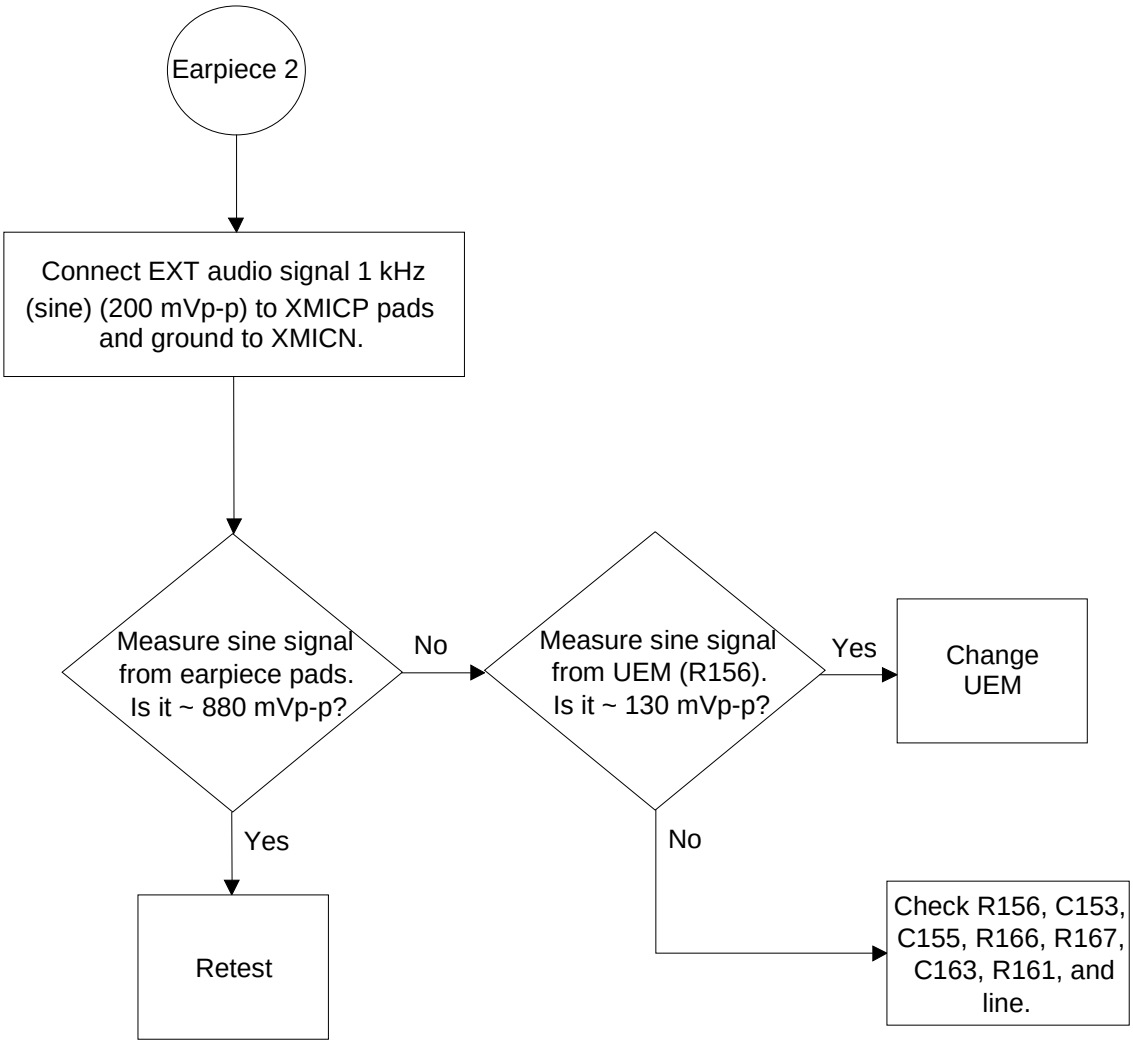
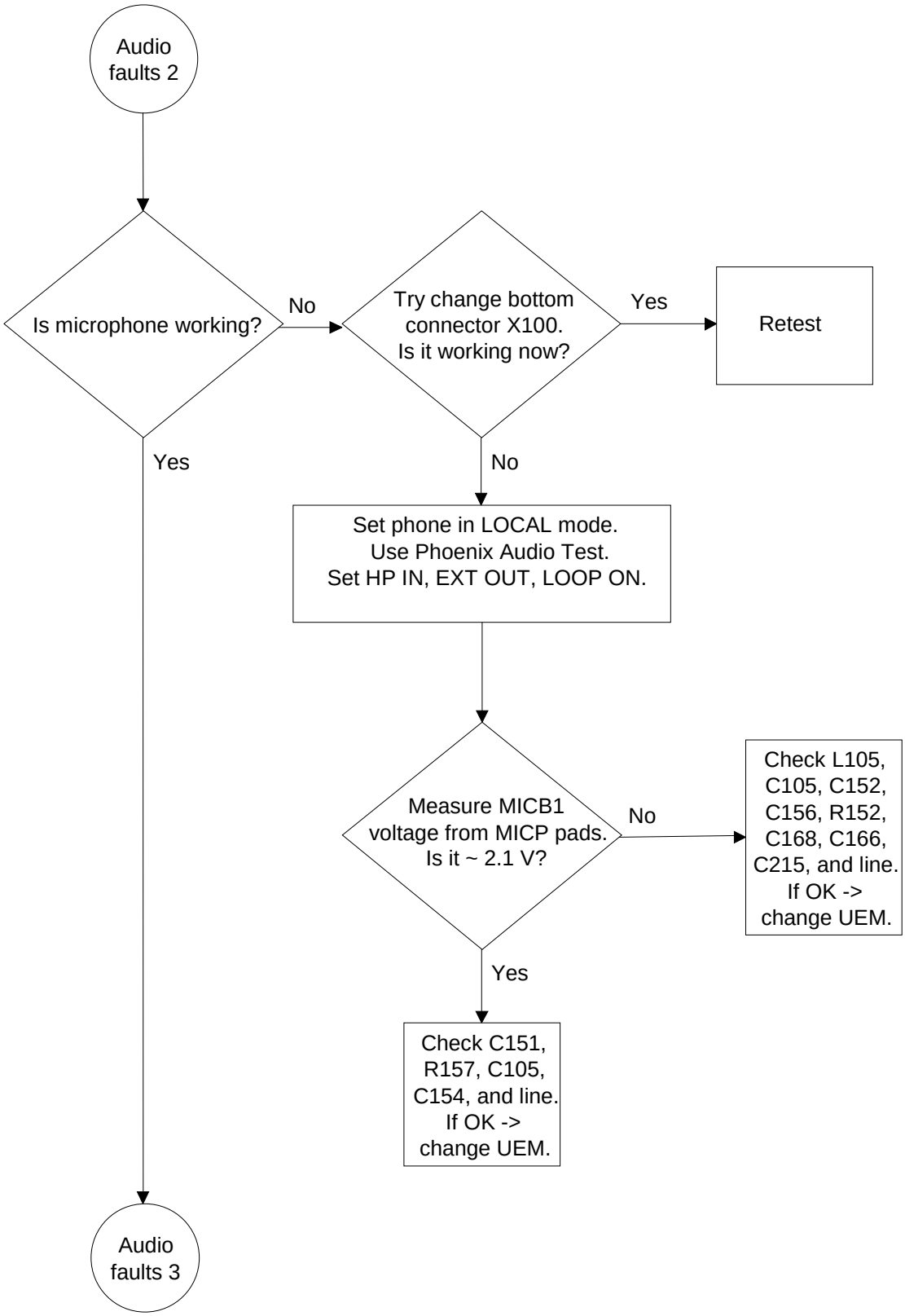


Figure 53: Audio Faults




Earpiece 2
Connect EXT audio signal 1 kHz (sine) (200 mVp-p) to XMICP pads and ground to XMICN.
Measure sine signal from earpiece pads. Is it ~ 880 mVp-p?
No
Measure sine signal from UEM (R156). Is it ~ 130 mVp-p?
Yes
Change UEM
Yes
Retest
No
Check R156, C153, C155, R166, R167, C163, R161, and line.


Audio faults 2
Is microphone working?
No
Try change bottom connector X100. Is it working now?
Yes
Retest
Yes
No
Set phone in LOCAL mode. Use Phoenix Audio Test. Set HP IN, EXT OUT, LOOP ON.
Measure MICB1 voltage from MICP pads. Is it ~ 2.1 V?
No
Check L105, C105, C152, C156, R152, C168, C166, C215, and line. If OK -> change UEM.
Yes
Check C151, R157, C105, C154, and line. If OK -> change UEM.
Audio faults 3

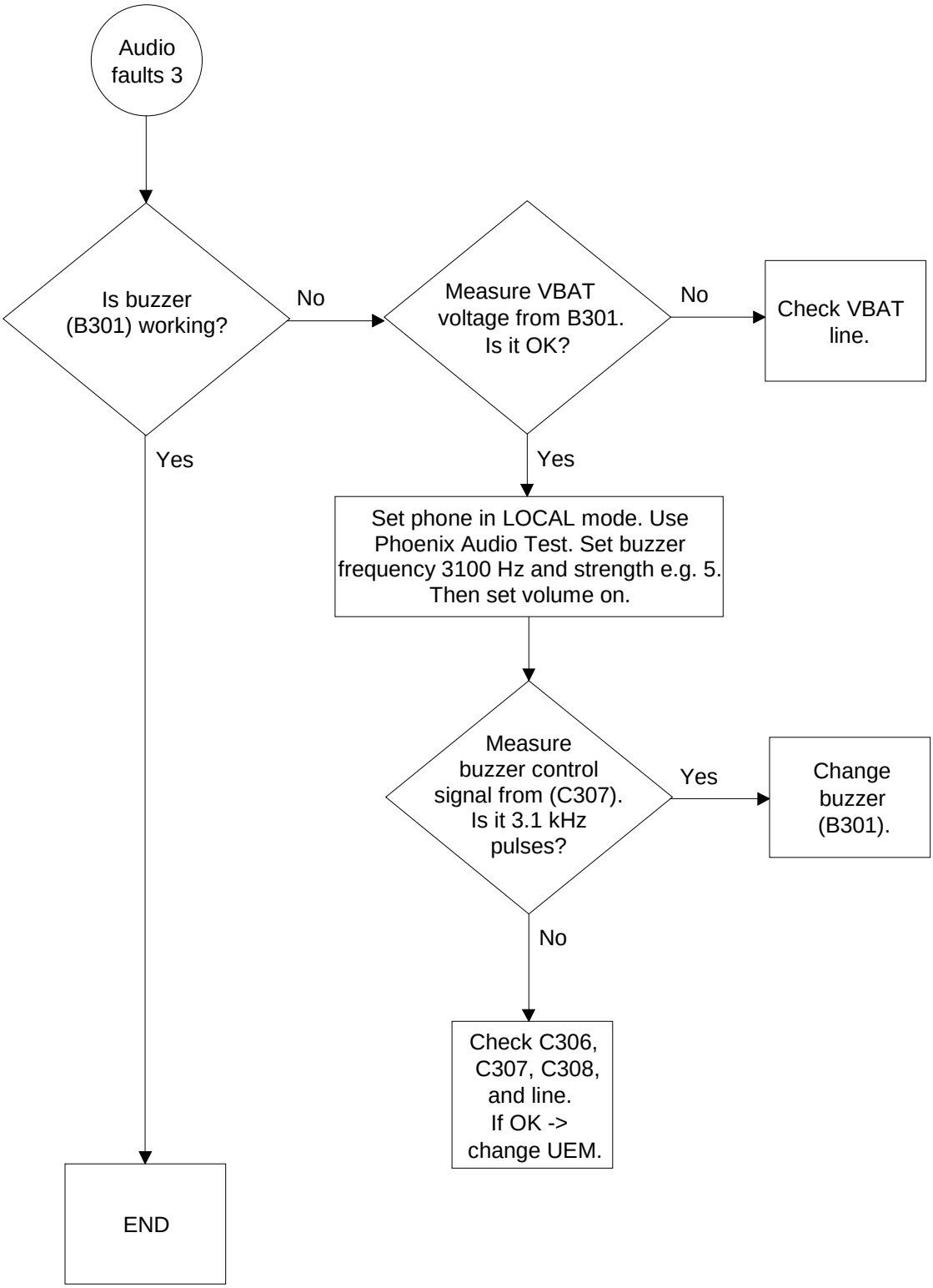
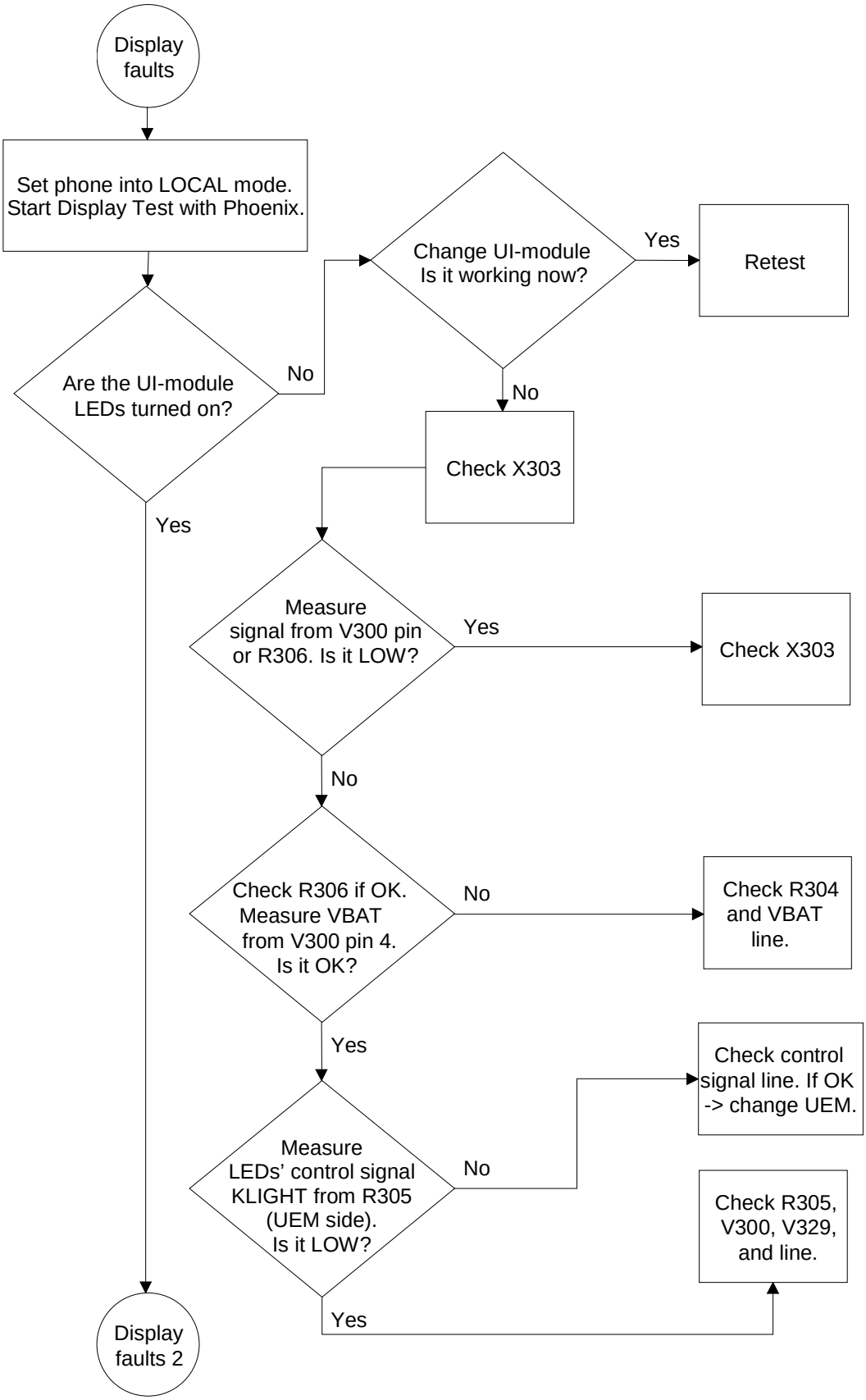
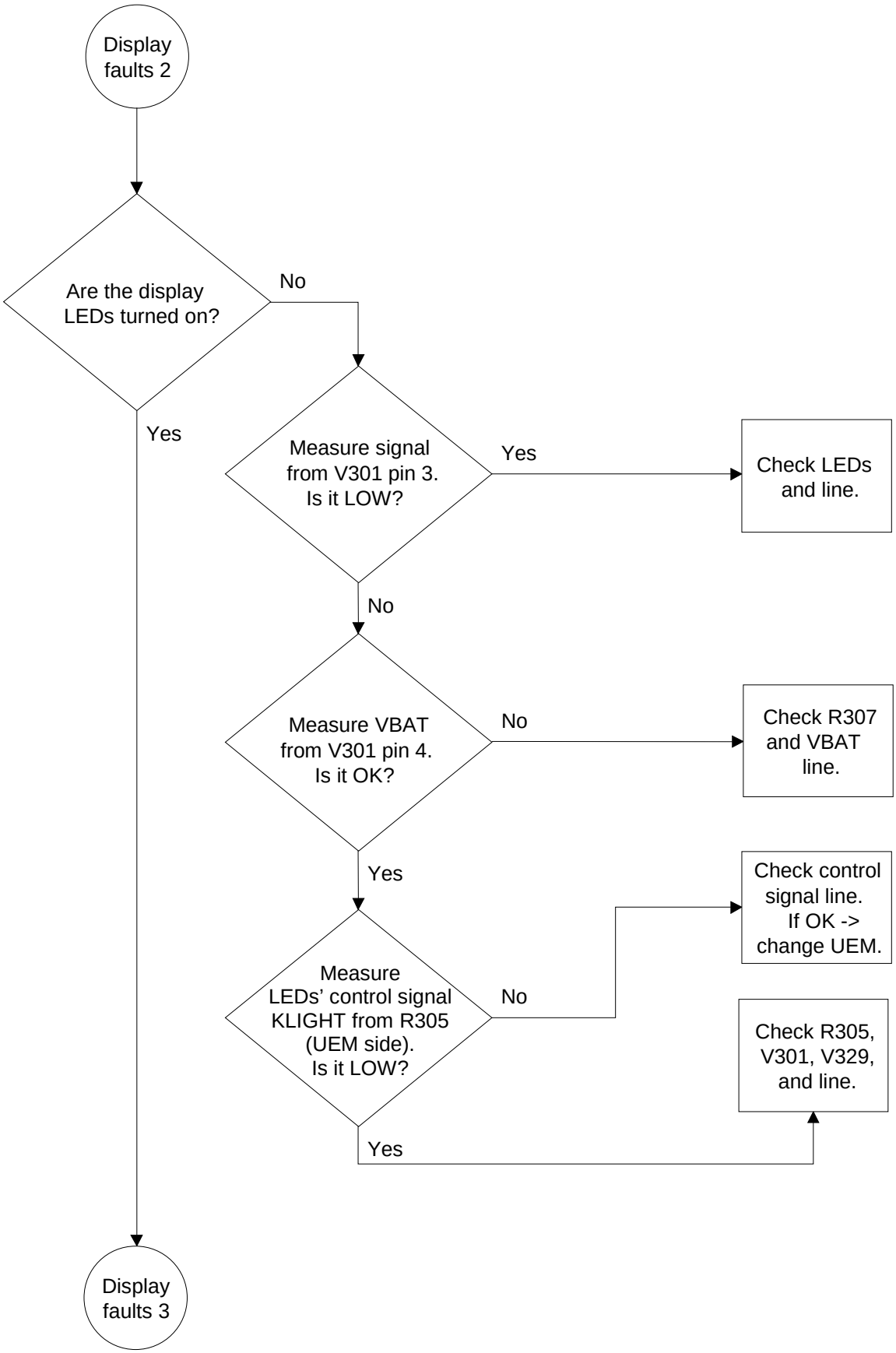

Audio faults 3
Is buzzer (B301) working?
No
Measure VBAT voltage from B301. Is it OK?
No
Check VBAT line.
Yes
Yes
Set phone in LOCAL mode. Use Phoenix Audio Test. Set buzzer frequency 3100 Hz and strength e.g. 5. Then set volume on.
Measure buzzer control signal from (C307). Is it 3.1 kHz pulses?
Yes
Change buzzer (B301).
No
Check C306, C307, C308, and line. If OK -> change UEM.
END

Figure 54: Display faults




Display faults 2
Are the display LEDs turned on?
No
Yes
Measure signal from V301 pin 3. Is it LOW?
Yes
Check LEDs and line.
No
Measure VBAT from V301 pin 4. Is it OK?
No
Check R307 and VBAT line.
Yes
Measure LEDs' control signal KLIGHT from R305 (UEM side). Is it LOW?
No
Check control signal line. If OK -> change UEM.
Check R305, V301, V329, and line.
Yes
Display faults 3

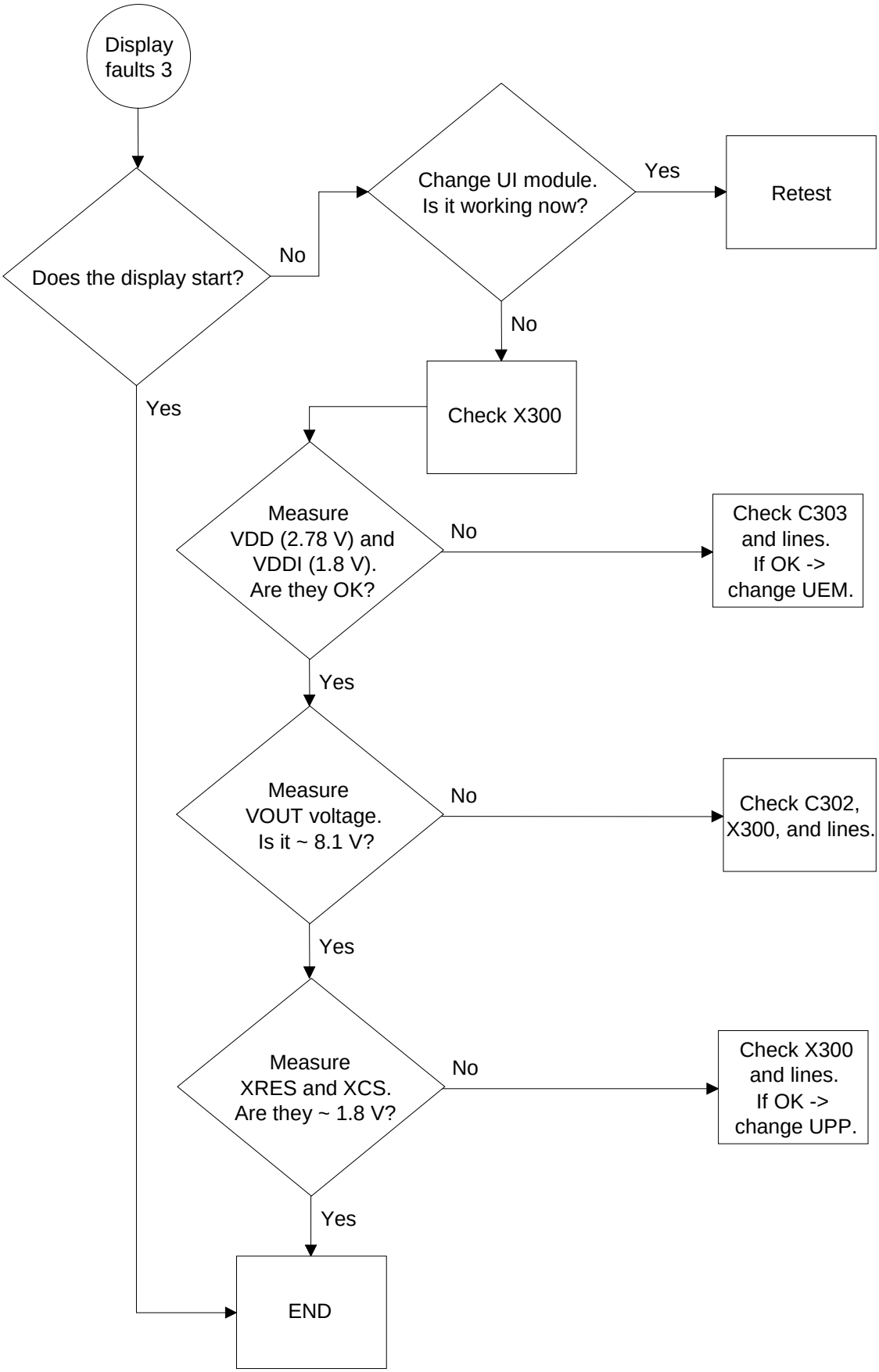
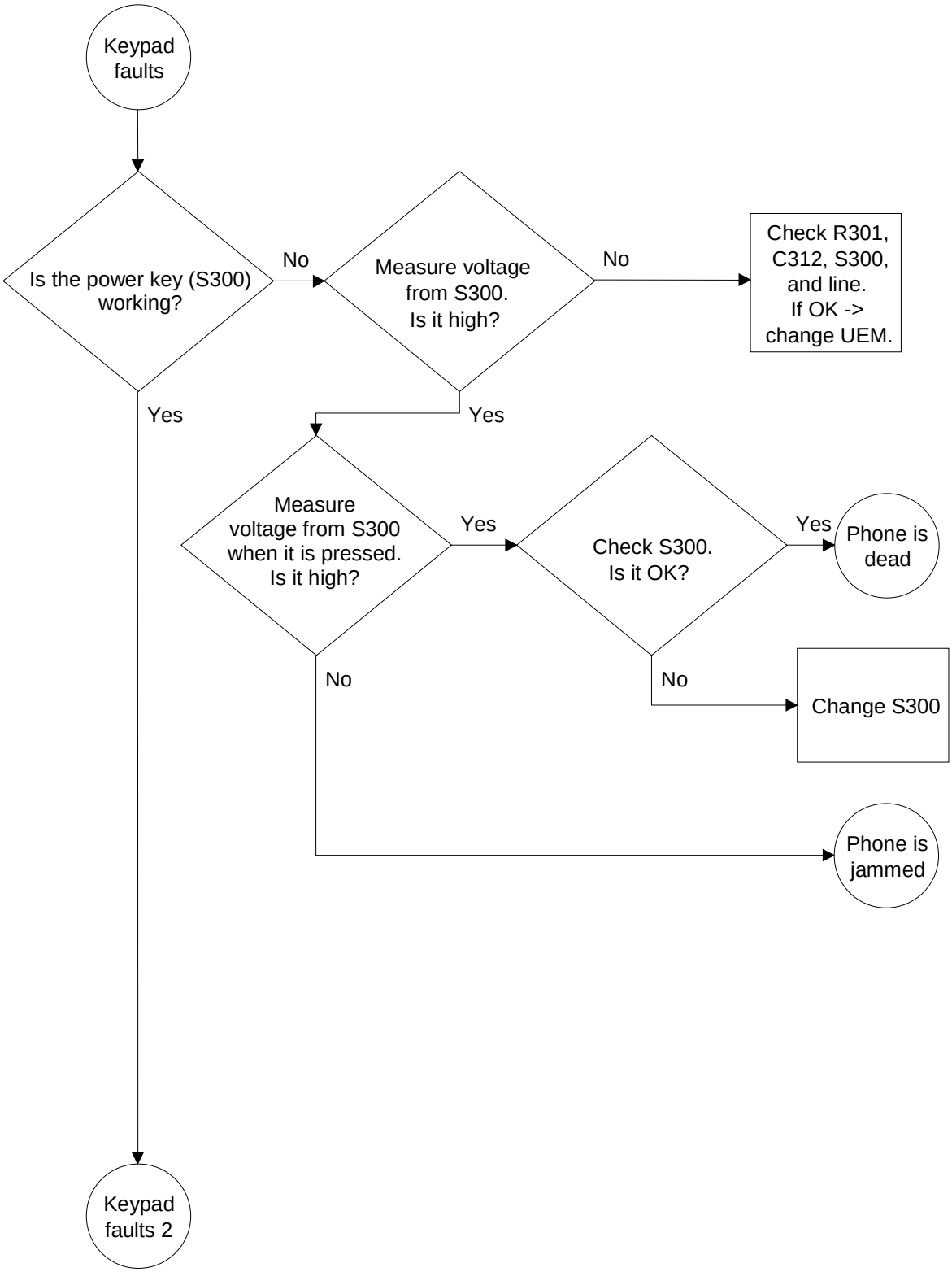
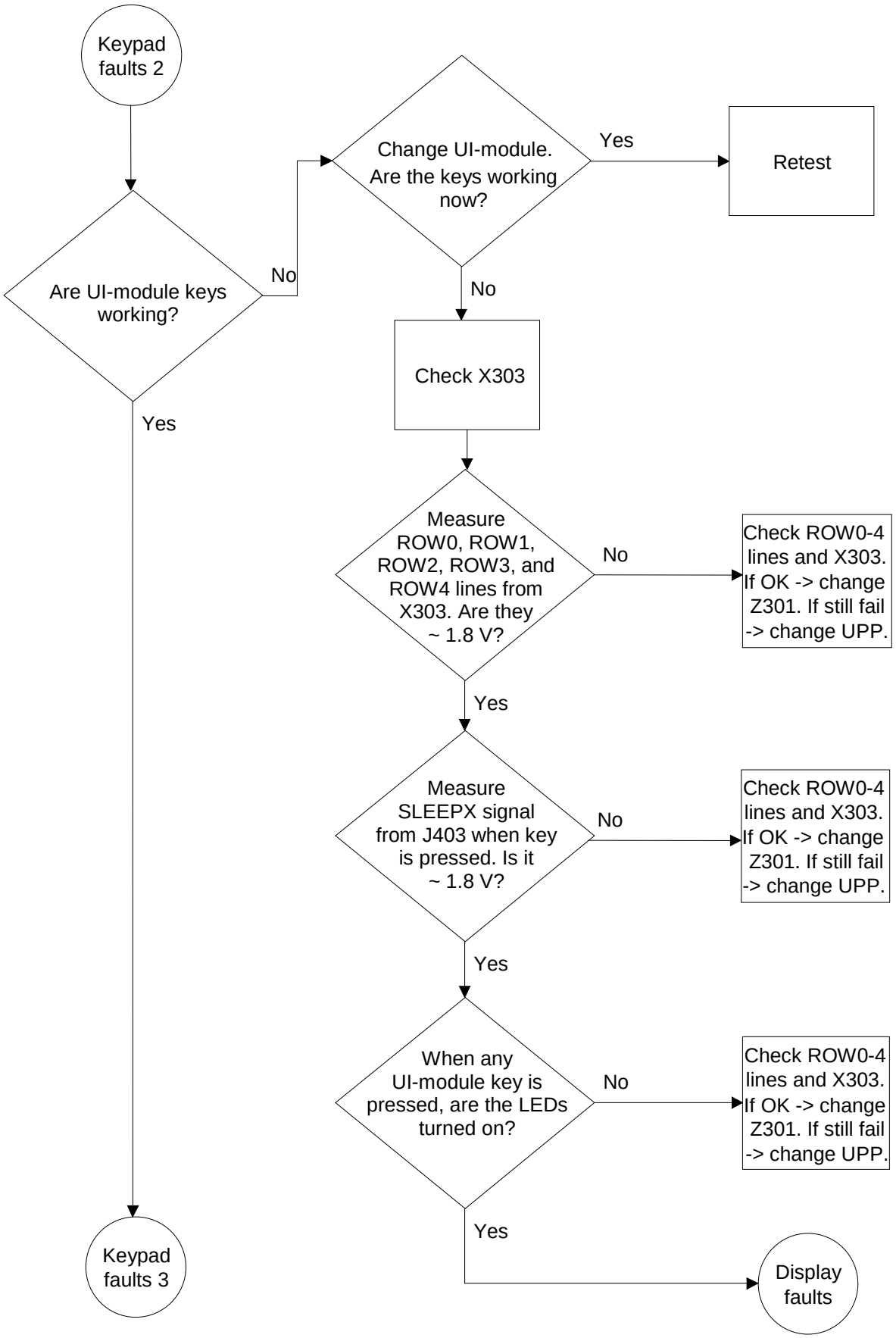
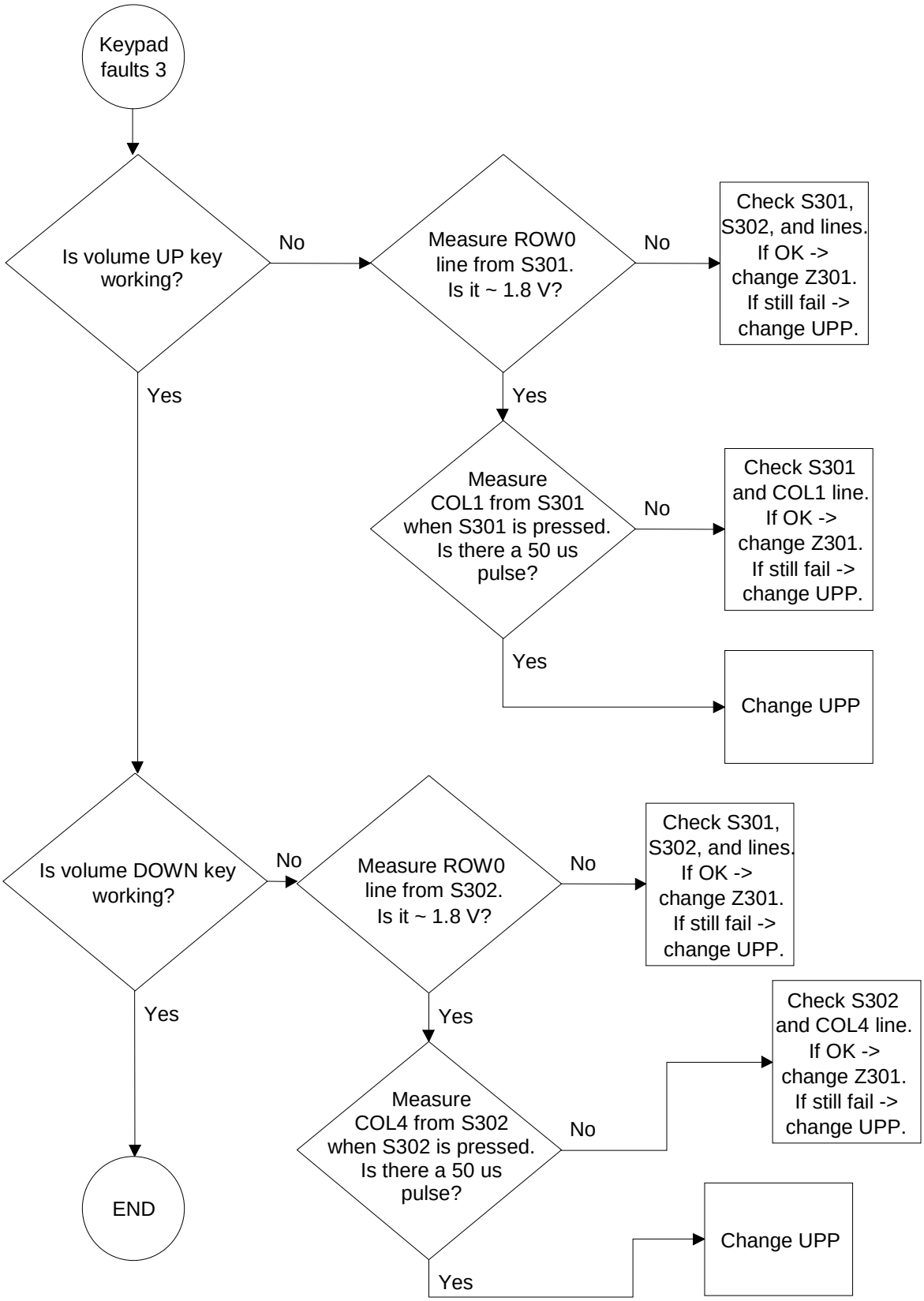

Display faults 3
Does the display start?
No
Change UI module. Is it working now?
Yes
Retest
No
Check X300
Yes
Measure VDD (2.78 V) and VDDI (1.8 V). Are they OK?
No
Check C303 and lines. If OK -> change UEM.
Yes
Measure VOUT voltage. Is it ~ 8.1 V?
No
Check C302, X300, and lines.
Yes
Measure XRES and XCS. Are they ~ 1.8 V?
No
Check X300 and lines. If OK -> change UPP.
Yes
END

Figure 55: Keypad Faults




Keypad faults 2
Are UI-module keys working?
No
Change UI-module. Are the keys working now?
Yes
Retest
No
Check X303
Yes
Keypad faults 3
Measure ROW0, ROW1, ROW2, ROW3, and ROW4 lines from X303. Are they ~ 1.8 V?
No
Check ROW0-4 lines and X303. If OK -> change Z301. If still fail -> change UPP.
Yes
Measure SLEEPX signal from J403 when key is pressed. Is it ~ 1.8 V?
No
Check ROW0-4 lines and X303. If OK -> change Z301. If still fail -> change UPP.
Yes
When any UI-module key is pressed, are the LEDs turned on?
No
Check ROW0-4 lines and X303. If OK -> change Z301. If still fail -> change UPP.
Yes
Display faults


Keypad faults 3
Is volume UP key working?
No
Measure ROW0 line from S301. Is it ~ 1.8 V?
No
Check S301, S302, and lines. If OK -> change Z301. If still fail -> change UPP.
Yes
Yes
Measure COL1 from S301 when S301 is pressed. Is there a 50 us pulse?
No
Check S301 and COL1 line. If OK -> change Z301. If still fail -> change UPP.
Yes
Change UPP
Is volume DOWN key working?
No
Measure ROW0 line from S302. Is it ~ 1.8 V?
No
Check S301, S302, and lines. If OK -> change Z301. If still fail -> change UPP.
Yes
Yes
Measure COL4 from S302 when S302 is pressed. Is there a 50 us pulse?
No
Check S302 and COL4 line. If OK -> change Z301. If still fail -> change UPP.
END
Yes
Change UPP

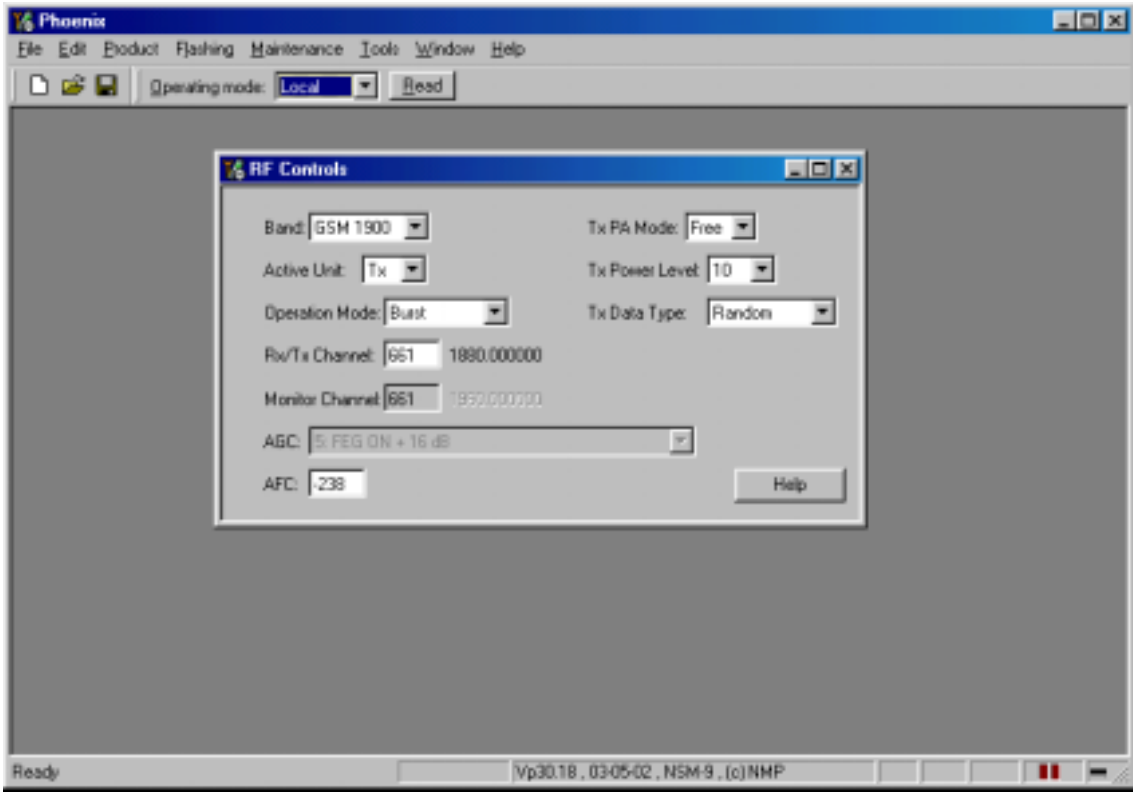
RF Troubleshooting Instructions

Issue 1 10/02

RF Troubleshooting

Phone settings for TX1900 Troubleshooting

TX – Burst mode
Channel 661
PCL10

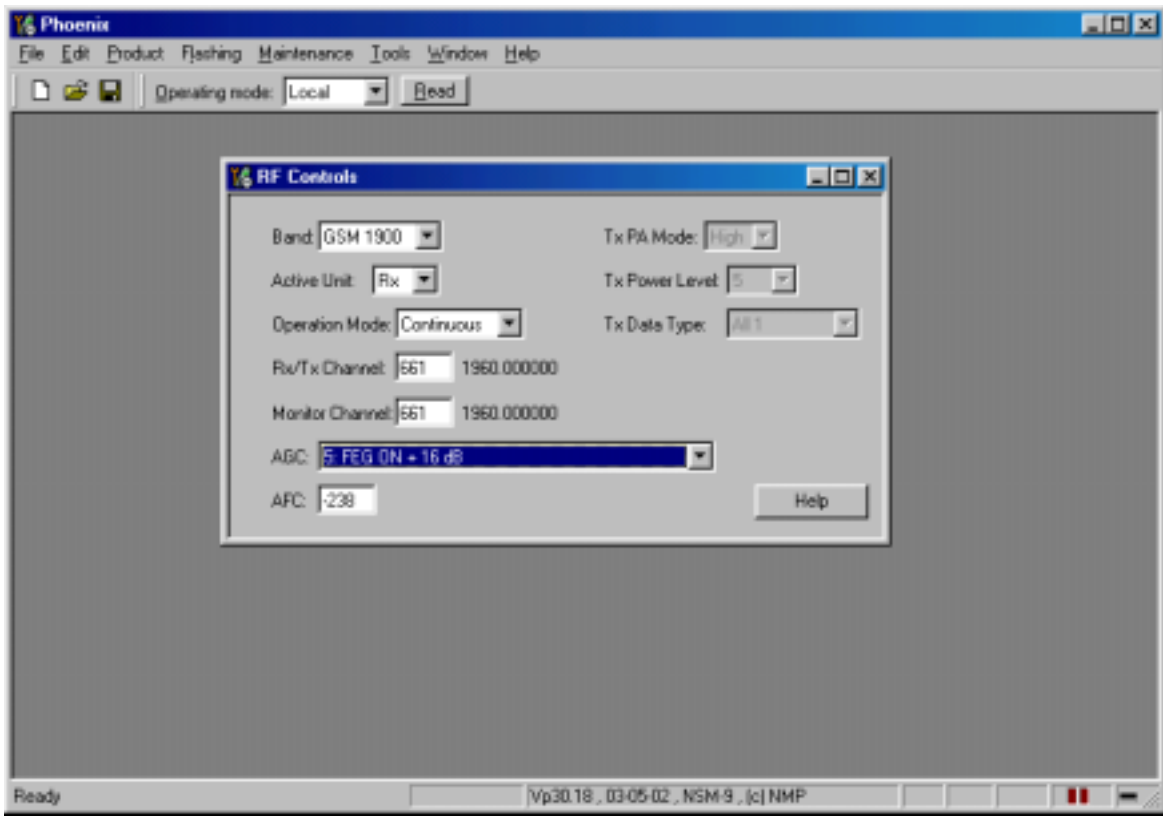


No TX GSM1900

1 Check 26 MHz VCTCXO at TP20 (Test Point 20). Frequency deviation should be <100 Hz). Check also TP3: Voltage should be 2.8VDC.
2 Check TX IQ signals at TP21. If not OK, change UEM.
3 Check 1880 MHz Ch661 at TP22. If OK, continue in step 8.
4 Check supply voltages for Hagar at TP4, TP5, TP6, TP8: 2.8 VDC; TP10 1.35 VDC and TP1 4.8VDC. If voltages are not OK, change UEM.
5 . Check SDATA at TP51, SCLK TP53, SLE TP52.
6 Check TXC at TP23
7 Check frequency of VCO in TP40 (3760 MHz/ ch 661, TX mode). If not OK, check TP7 2.8 VDC and TP41 ~2.8VDC. If TP41 is 4.8 VDC, the VCO doesn't probably work. If all Hagar input signals are OK, probably HAGAR is broken -> Change Hagar N600.
8 Check 1880 MHZ at TP25. If not OK, check Vbatt at TP9 3.9 VDC. Also check TP26. If TP9 and TP26 are OK, PA is probably broken -> Change PA N700.
9 Check 1880 MHz at TP30. If not OK, check TP28. Also check TP 29 squarevawe 2.8 Vpp at burst mode. If TP28 and TP29 are OK, change Z500 (antenna switch)

Phone settings for RX1900 Troubleshooting

RX- continuous mode
Channel 661
AGC value 5
+ signal generator feeds –55 dBm to antenna pad

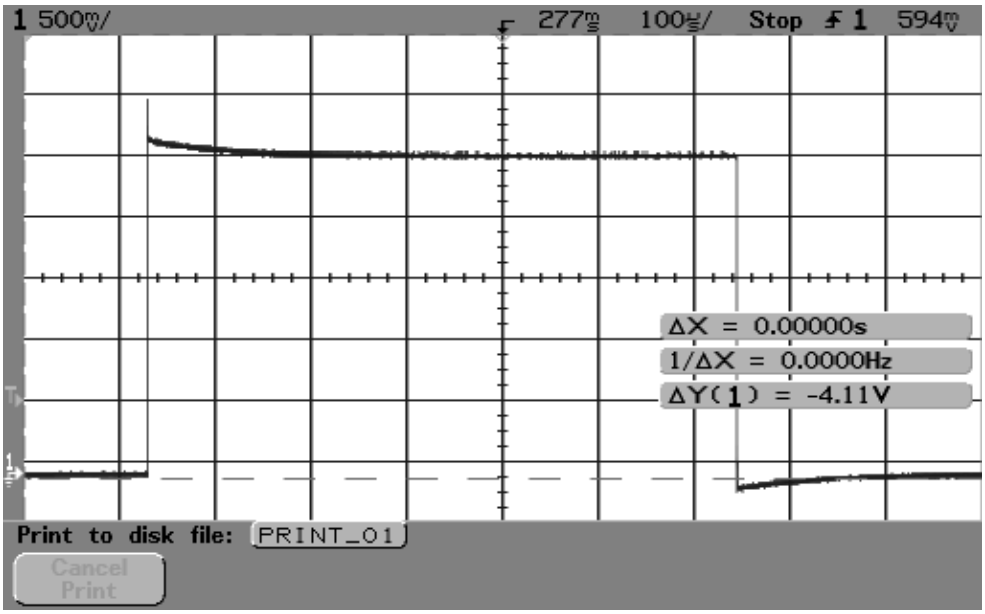


No RX GSM1900

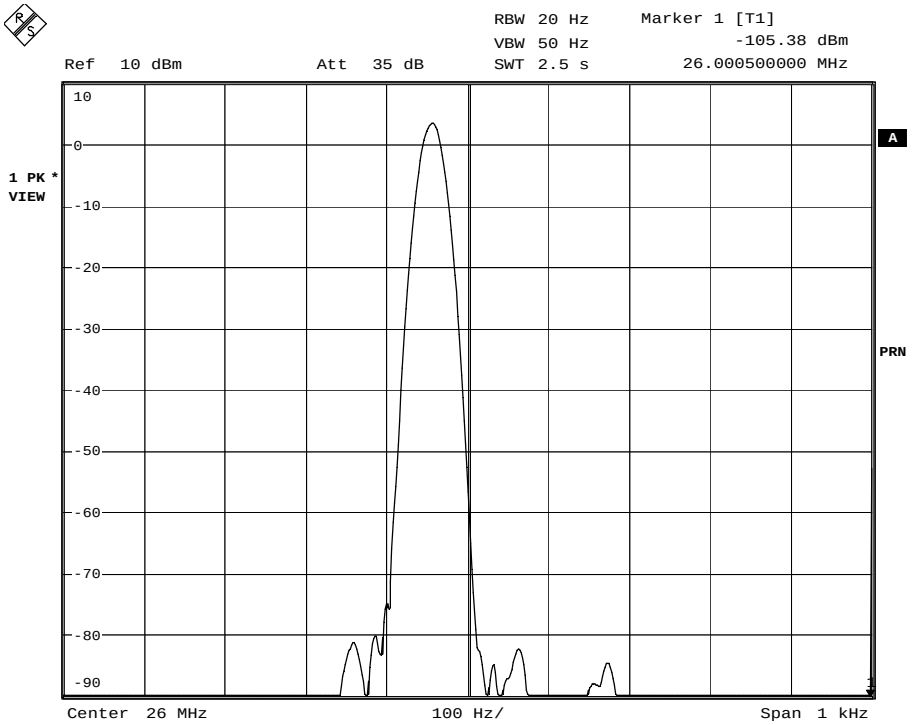
1 Check 26 MHz VCTCXO at TP20 (Test Point 20). Frequency deviation should be <100 Hz). Check also TP3: Voltage should be 2.8VDC.
2 Check RX signal level 1960 MHz at TP31. If not OK, change Z500
3 Check RX signal level at TP32. If not OK, change Z520.
4 Check RX signal level at TP33. If not OK, check voltages at TP33 2.7 VDC, TP34 2.7 VDC, TP35 0VDC. If TP 33 not OK, check L550 and R550. If components are OK, change V550. If that doesn't help change HAGAR N600.
5 Check RX signal level at TP36. If not OK, change Z551.
6 Check RX IQ signals at TP37 (also in burst-mode). If not OK, check HAGAR supply voltages at TP4, TP5, TP6, TP8: 2.8VDC. TP10 1.35VDC and TP1 4.8 VDC. If the voltages are not OK, change UEM.
7 Check SDATA at TP51, SCLK TP53 and SLE TP52.
8 Check frequency of VCO G650 at TP40 (3920 MHz/ CH661, RX cont mode). If not OK, check TP7 2.8 VDC and TP41 ~2.9VDC. If TP41 is 4.8 VDC, the VCO doesn't probably work. If all HAGAR input signals are OK, then HAGAR is probably broken -> change Hagar N600.
9 If all signal and voltage levels are OK -> change UEM.

Measurement points for AMS and production repair

TP29: Antenna switch control voltage

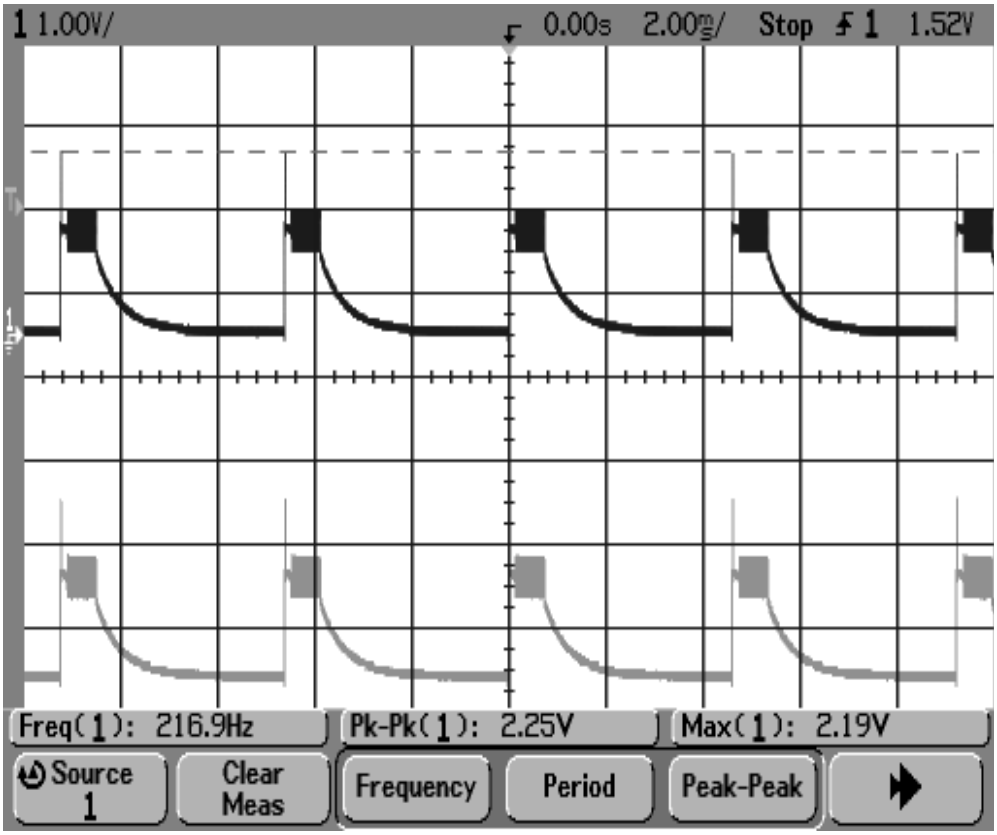


TP20: VCTCXO frequency

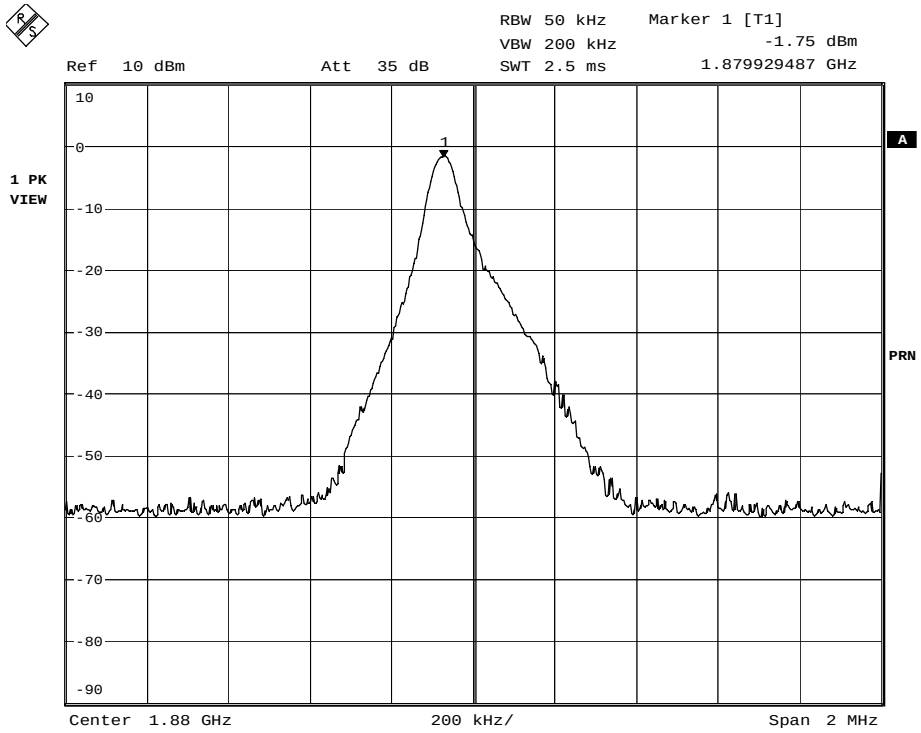


Comment A: TP63
Date: 4.APR.2002 10:09:44

TP21: TX I/Q

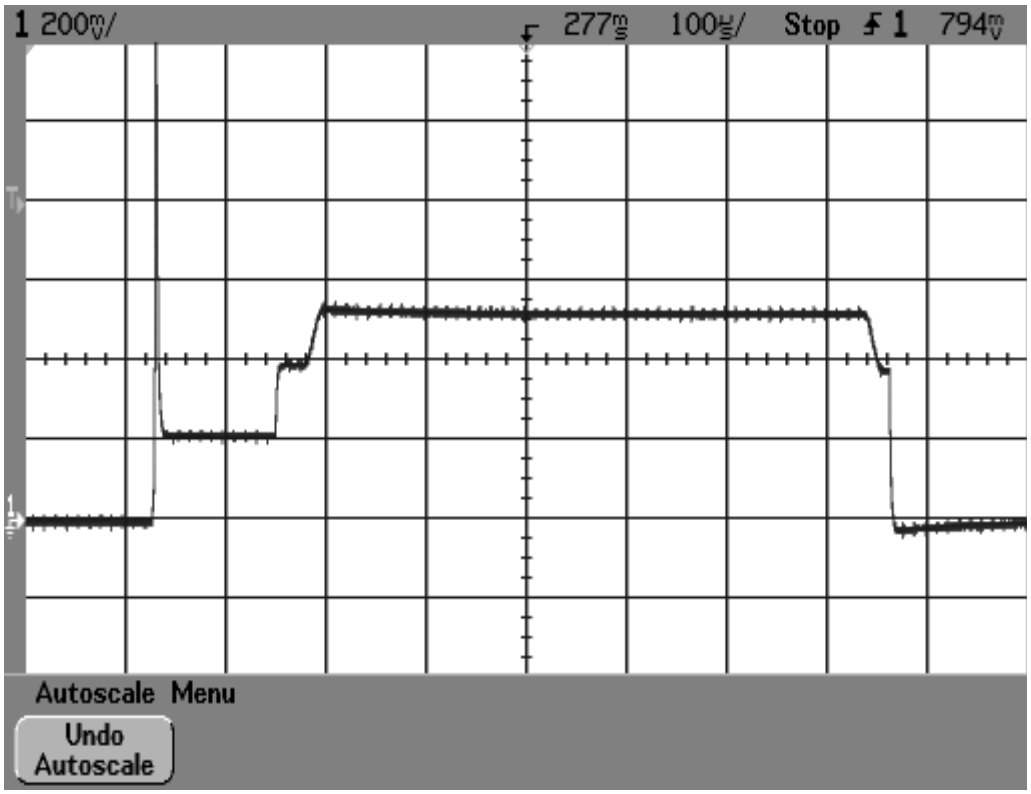


TP22: Hagar TX output 1900

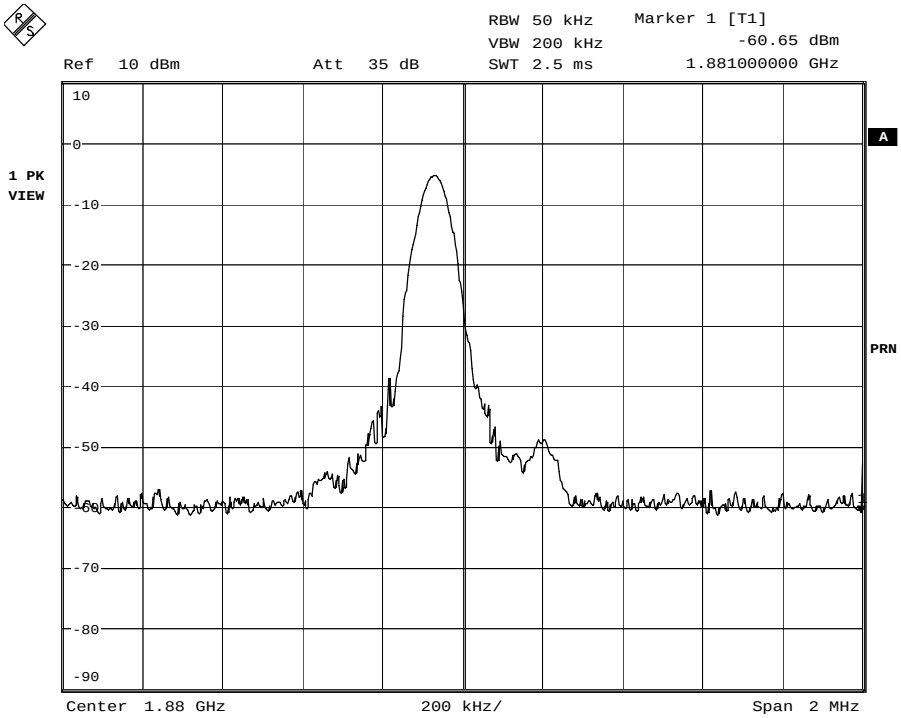


Comment A: TP63
Date: 4.APR.2002 10:31:24

TP23:TXC

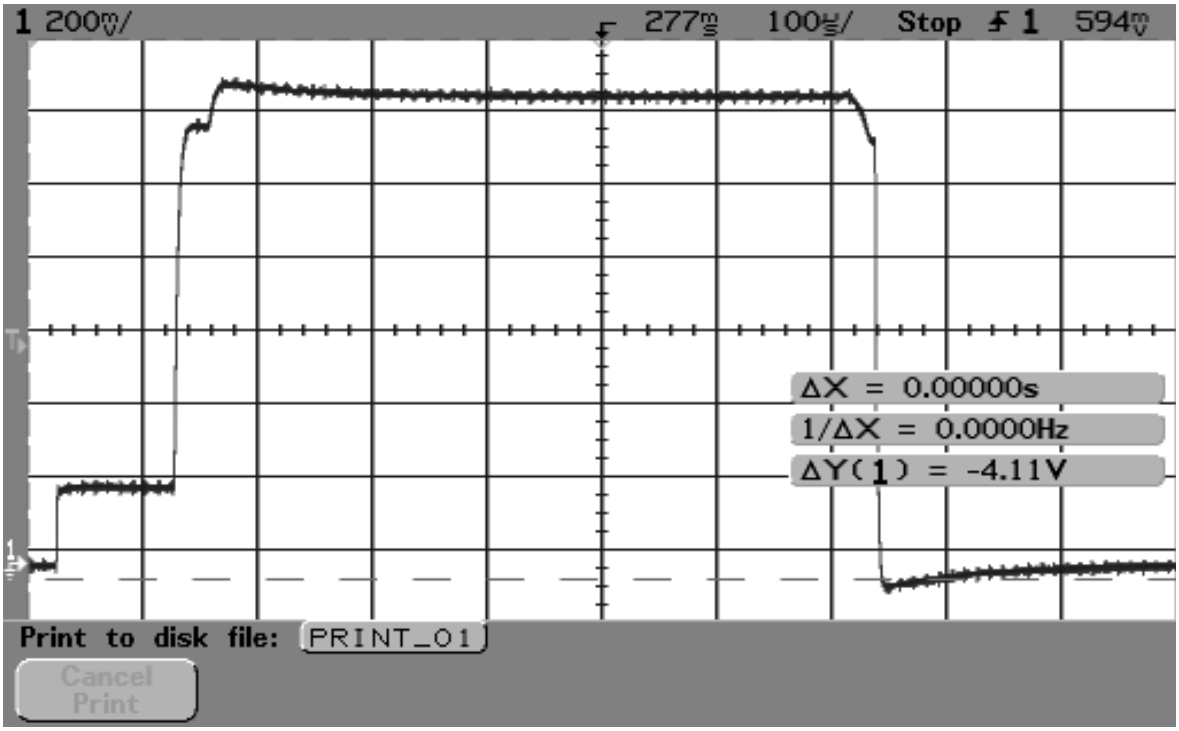


TP25:PA output 1900

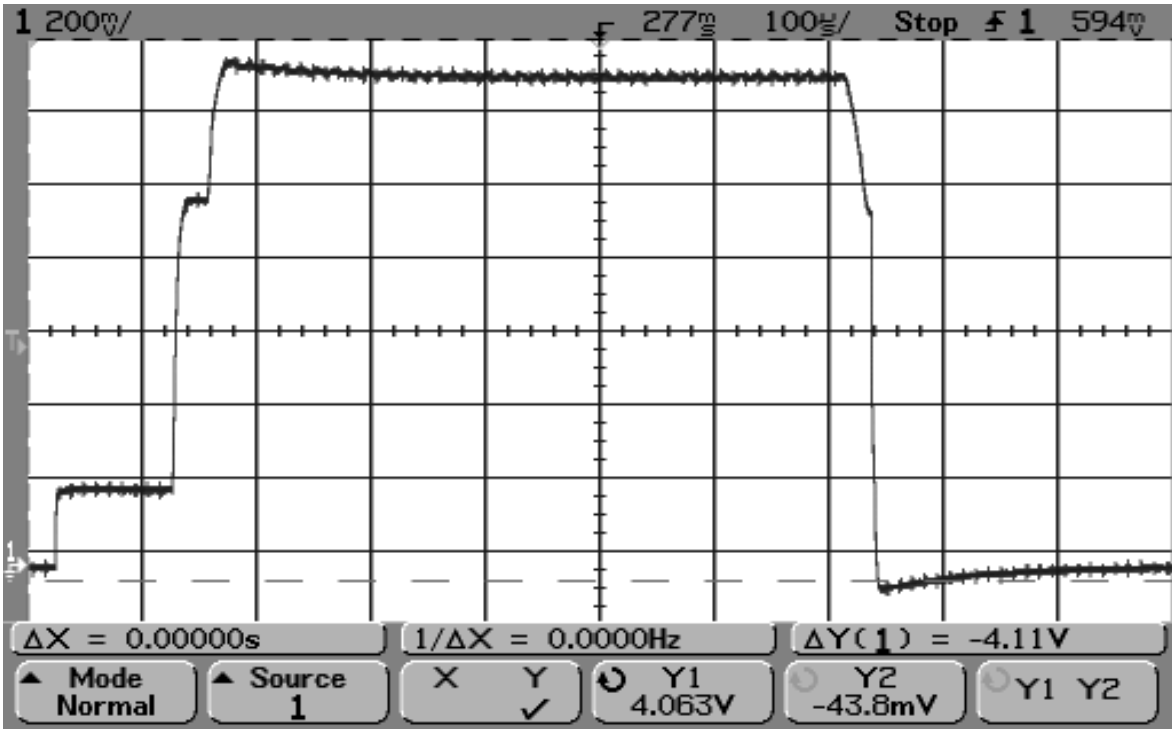


Comment A: TP63
Date: 4.APR.2002 11:27:31

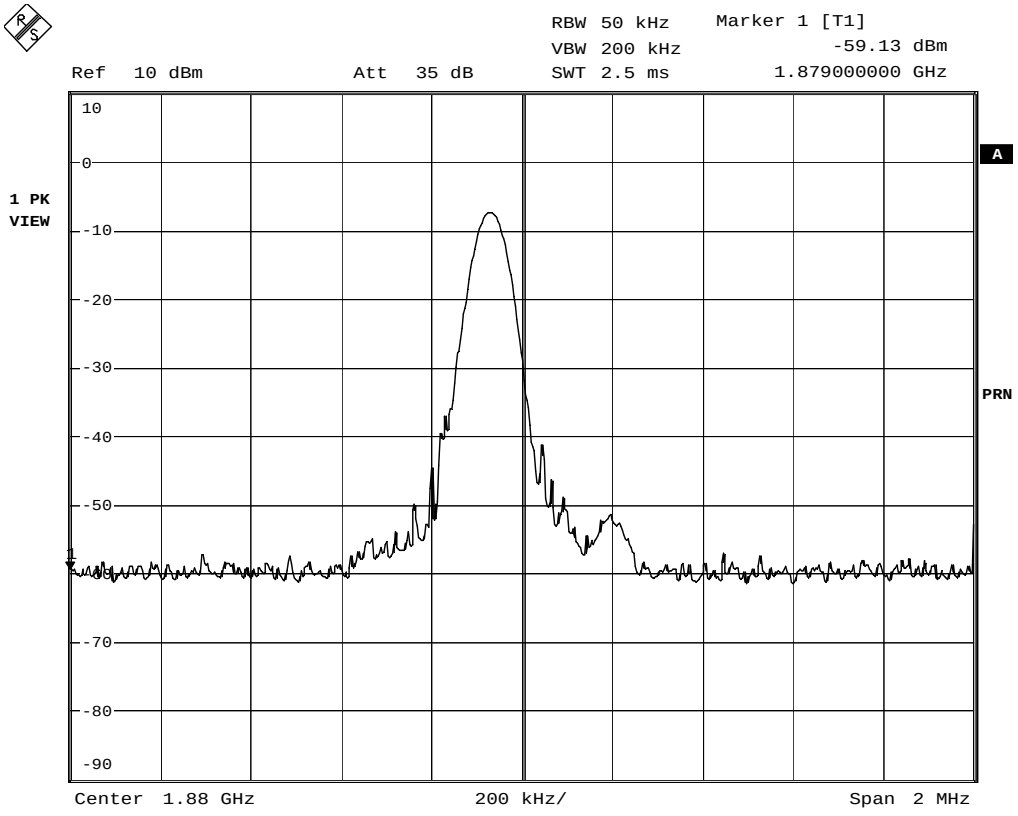
TP 26:V pctrl 1900



TP27:

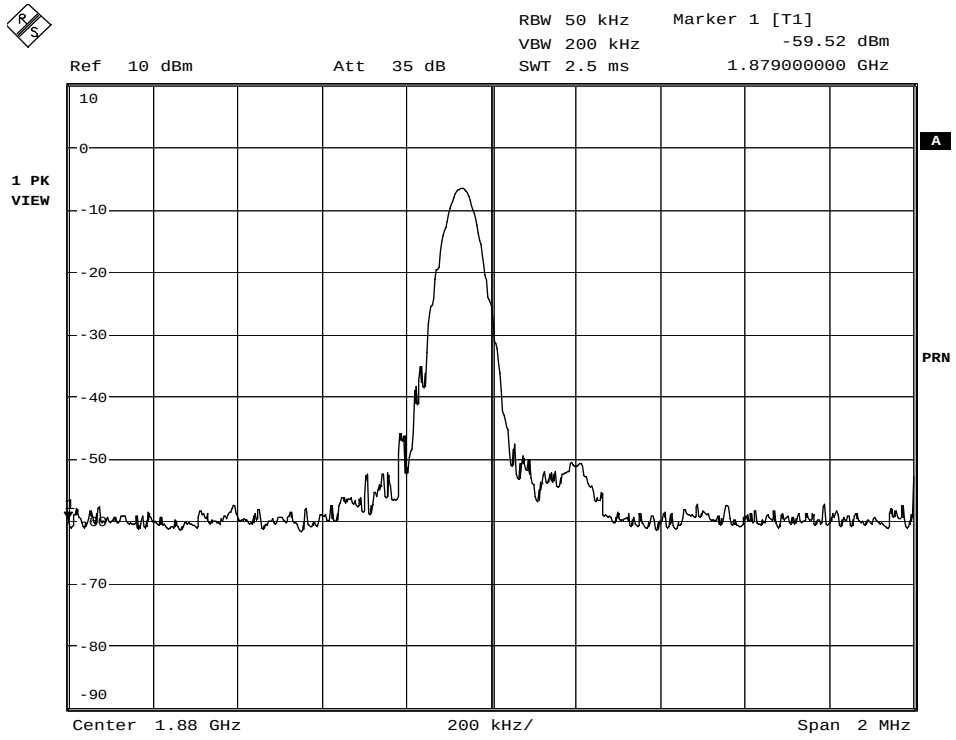


TP 28:



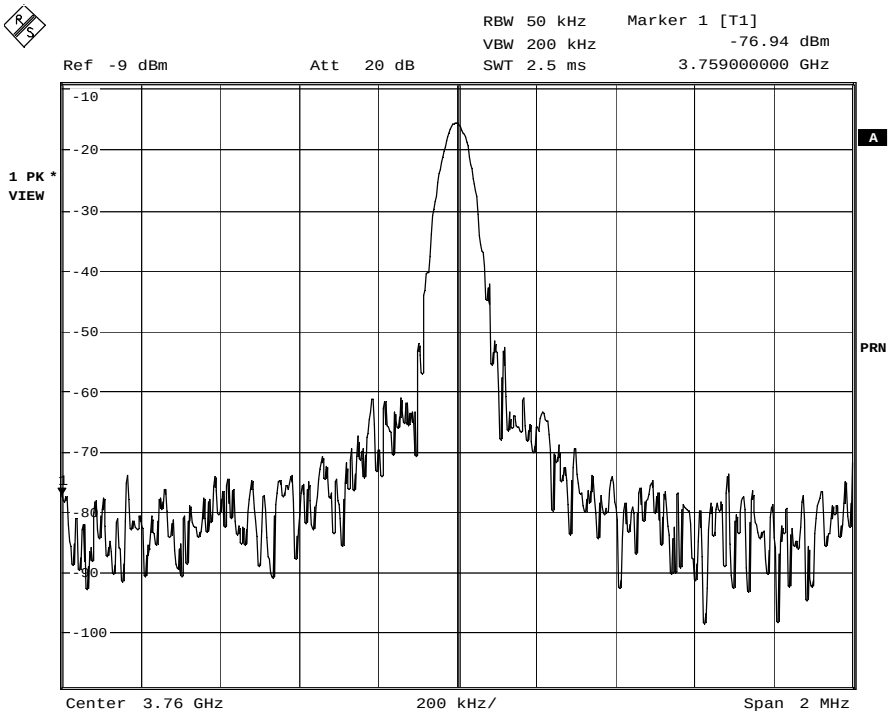
Comment A: TP63
Date: 4.APR.2002 11:43:27

TP30: 1900 TX:



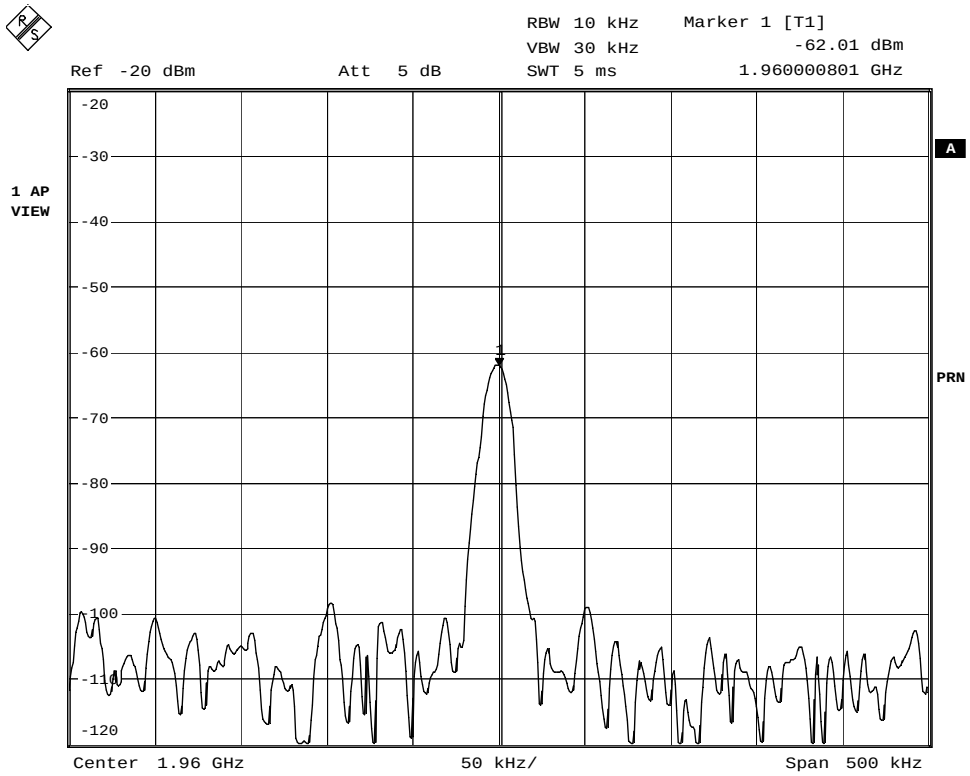
Comment A: TP63
Date: 4.APR.2002 11:40:53

TP40:1900MODE VCO frequency (mid ch)



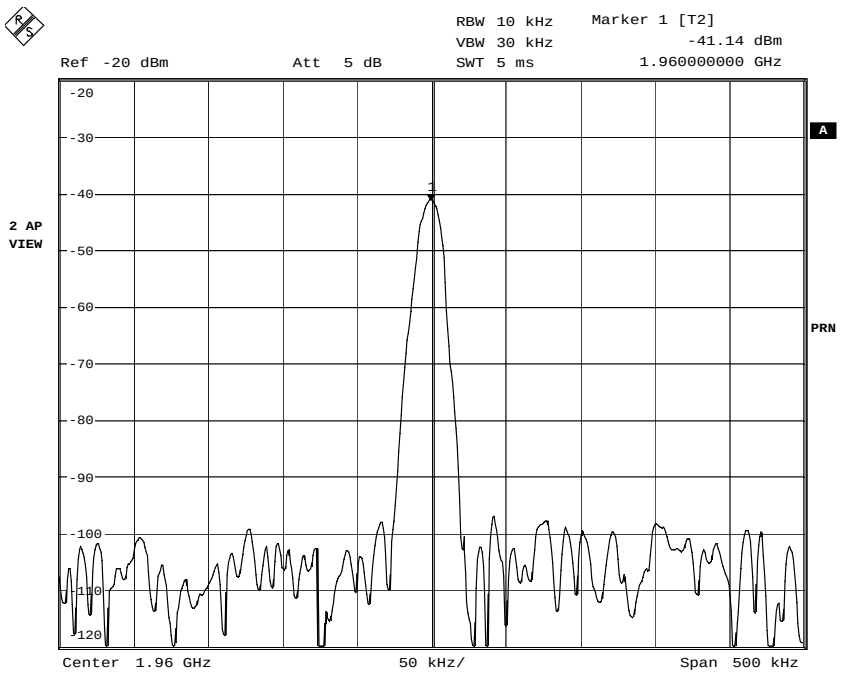
Comment A: TP63
Date: 4.APR.2002 11:14:26

TP31: Antenna switch RX output 1900



Comment A: TP63
Date: 4.APR.2002 09:30:54

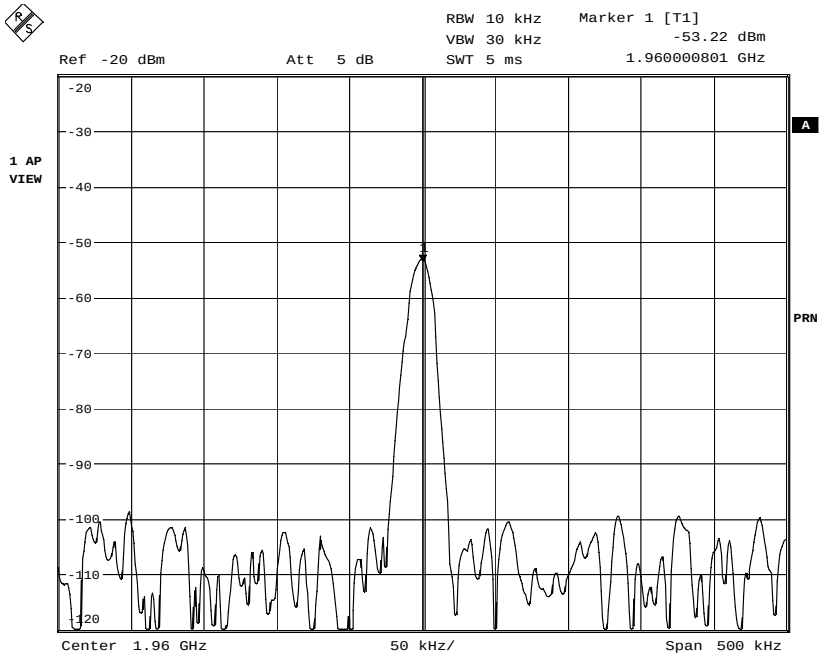
TP33: 1900 LNA output



Comment A: TP63
Date: 4.APR.2002 09:32:09

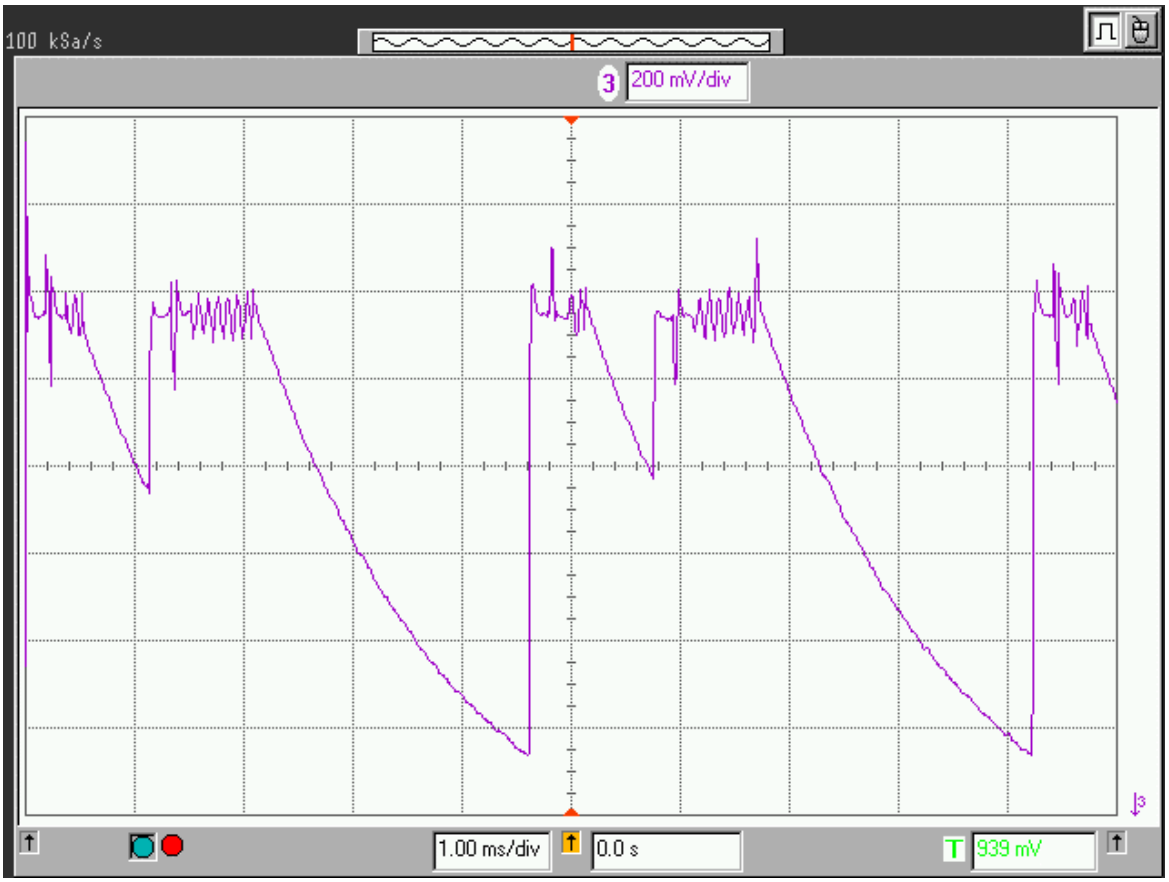
TP34, TP35 LNA voltages

TP36: 1900 RX Balanced SAW filter output

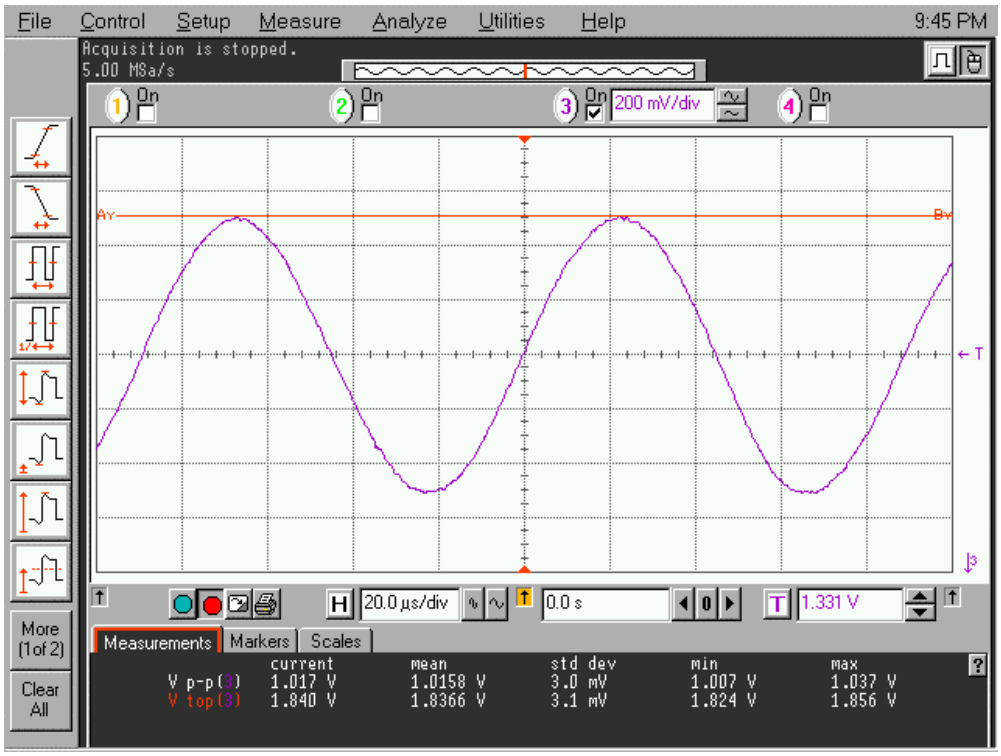


Comment A: TP63
Date: 4.APR.2002 09:33:27

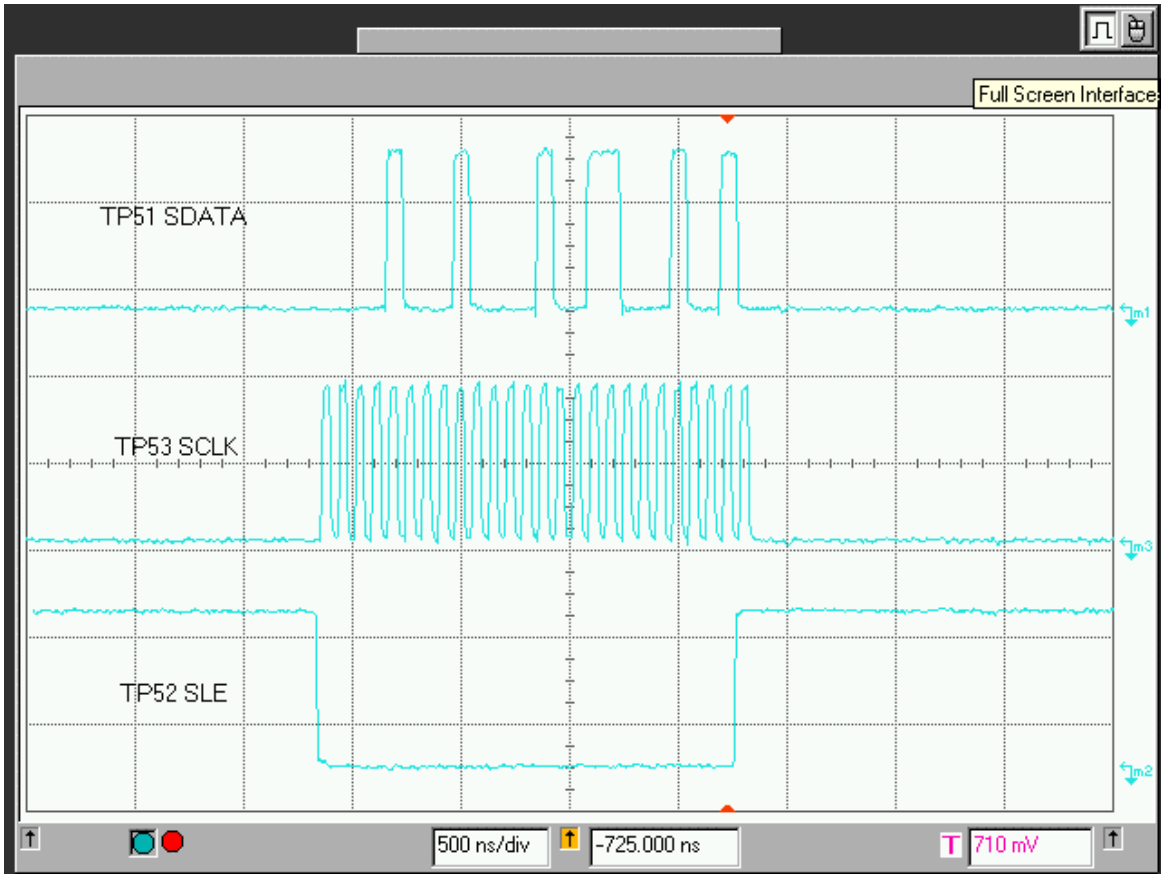
TP37 BURST MODE: RX I/Q

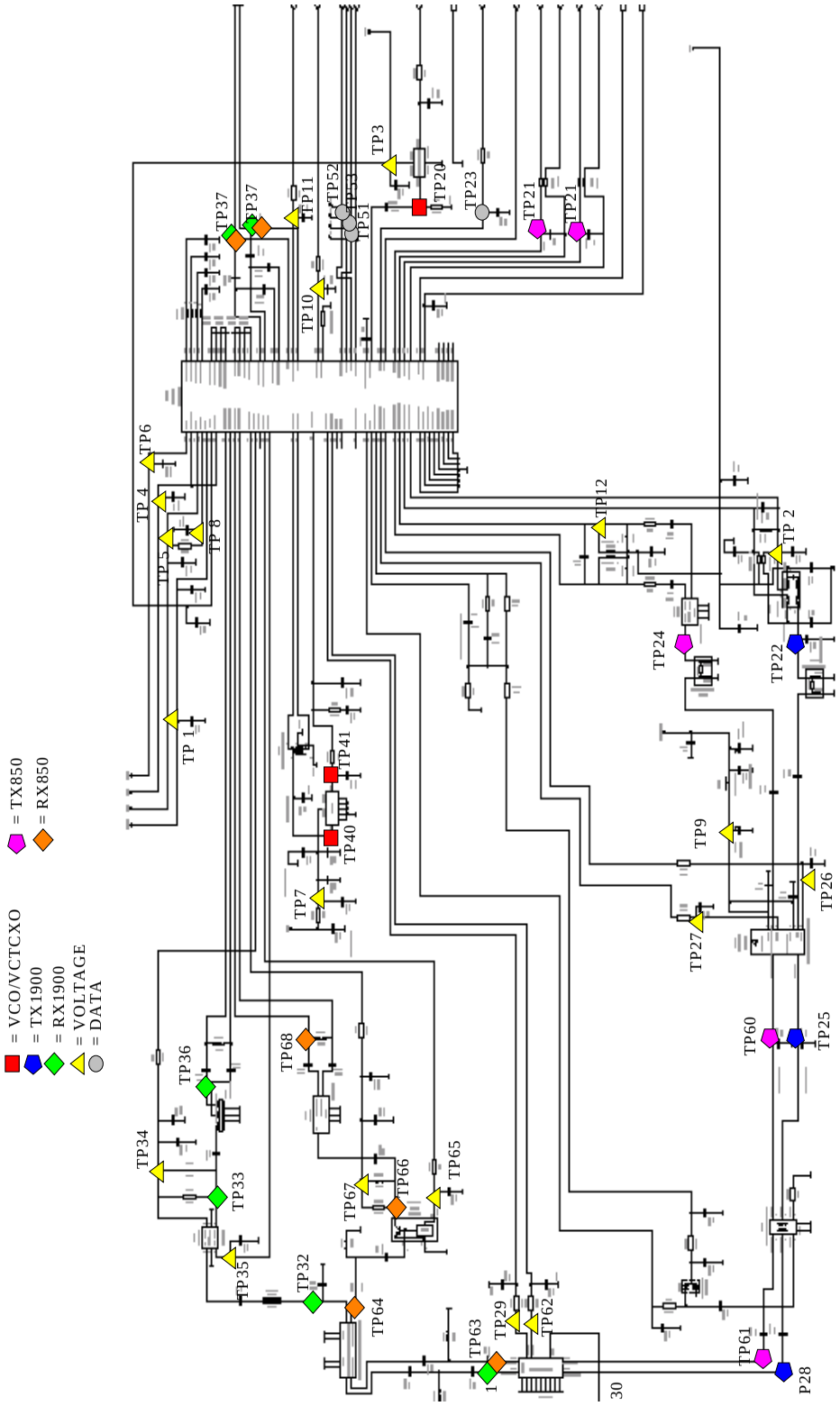


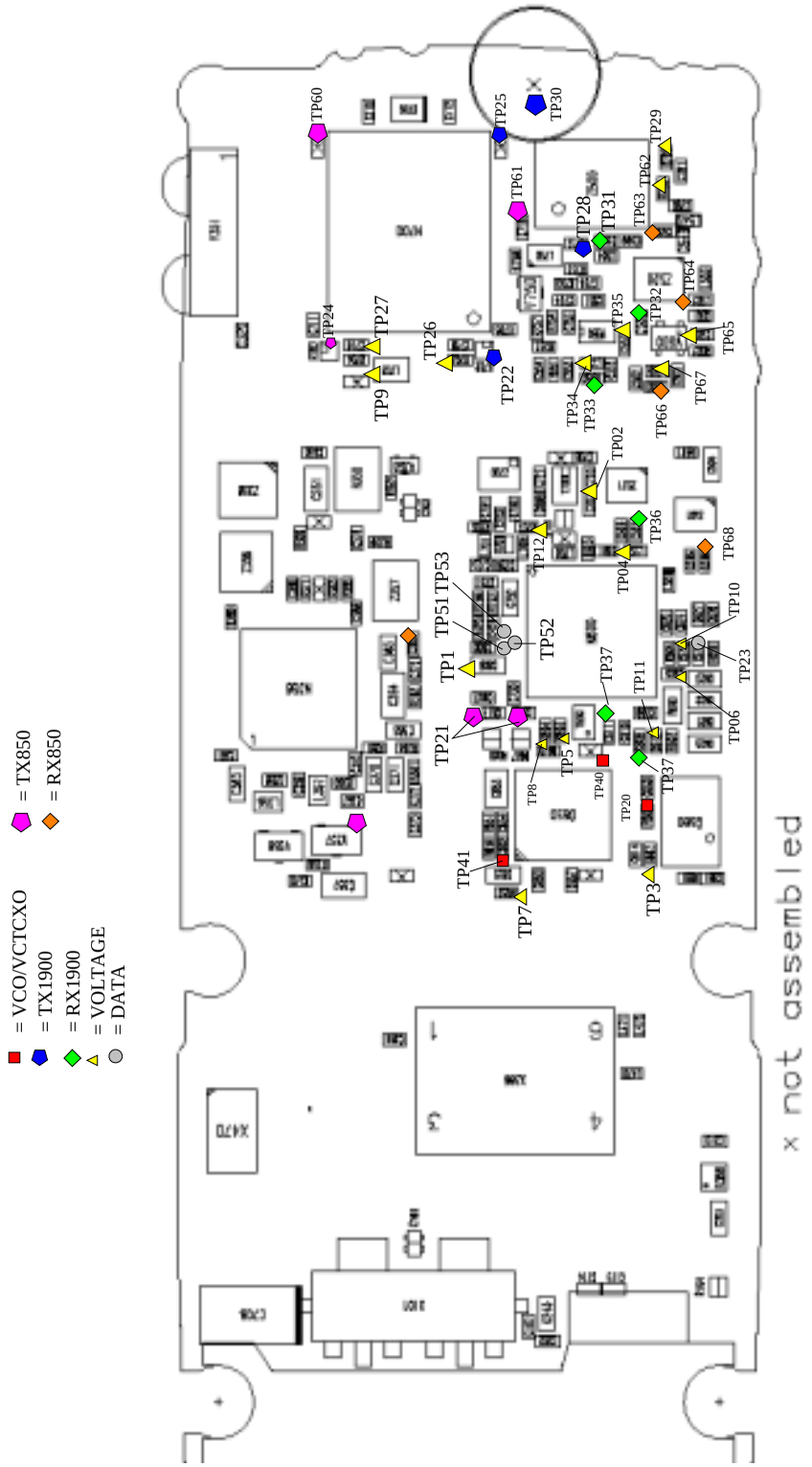
TP37 CONT MODE: RX I/Q



TP 51,52,53, 1900 MODE

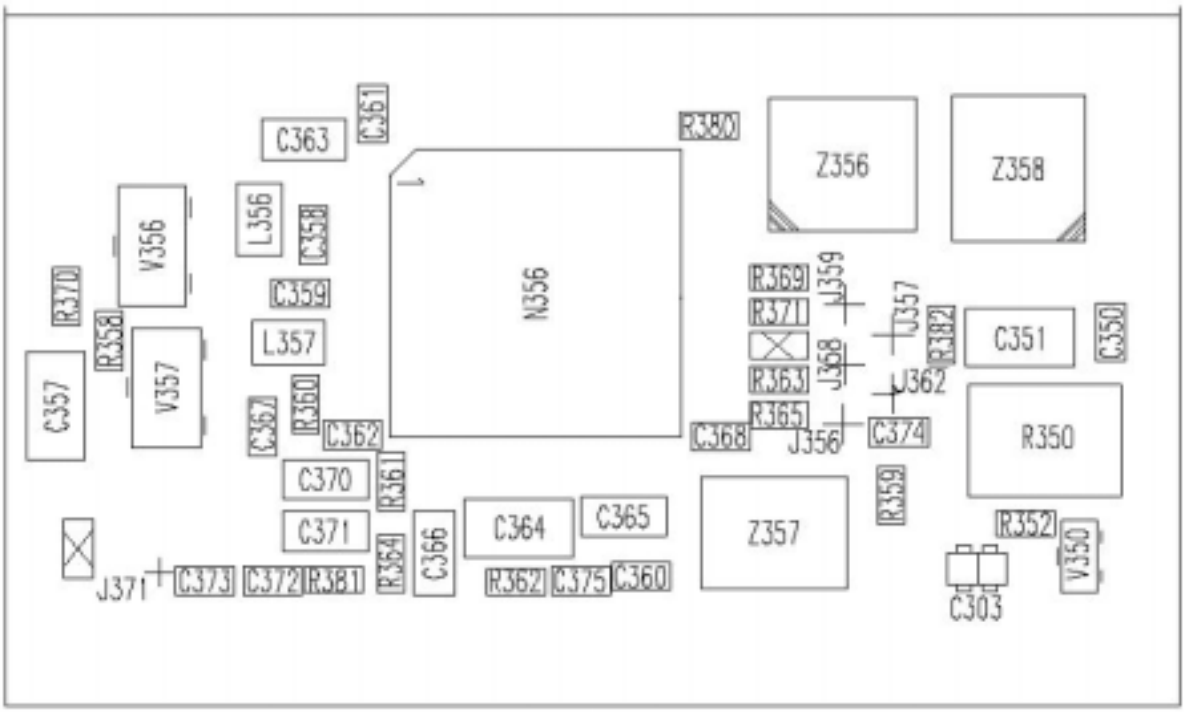



= VCO/VCTCXO
= TX1900
= RX1900
= VOLTAGE
= DATA
= TX850
= RX850
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP20
TP21
TP22
TP23
TP24
TP25
TP26
TP27
TP28
TP29
TP32
TP33
TP34
TP35
TP36
TP37
TP40
TP41
TP51
TP52
TP53
TP60
TP61
TP62
TP63
TP64
TP65
TP66
TP67
TP68
1
30


= TX850
= RX850
= VCO/VCTCXO
= TX1900
= RX1900
= VOLTAGE
= DATA
x not assembled
TP60
TP25
TP30
TP61
TP28
TP31
TP29
TP62
TP63
TP64
TP24
TP27
TP26
TP35
TP32
TP65
TP9
TP22
TP34
TP33
TP66
TP67
TP02
TP36
TP68
TP12
TP04
TP53
TP51
TP52
TP10
TP1
TP37
TP11
TP23
TP21
TP5
TP06
TP8
TP40
TP20
TP37
TP41
TP3
TP7

FM Radio Troubleshooting

Figure 1: FM radio component layout.



Components L101, C101 and C102 are not shown in picture 1. Components are placed in baseband section.

"X "–marked components are non-assembled components.

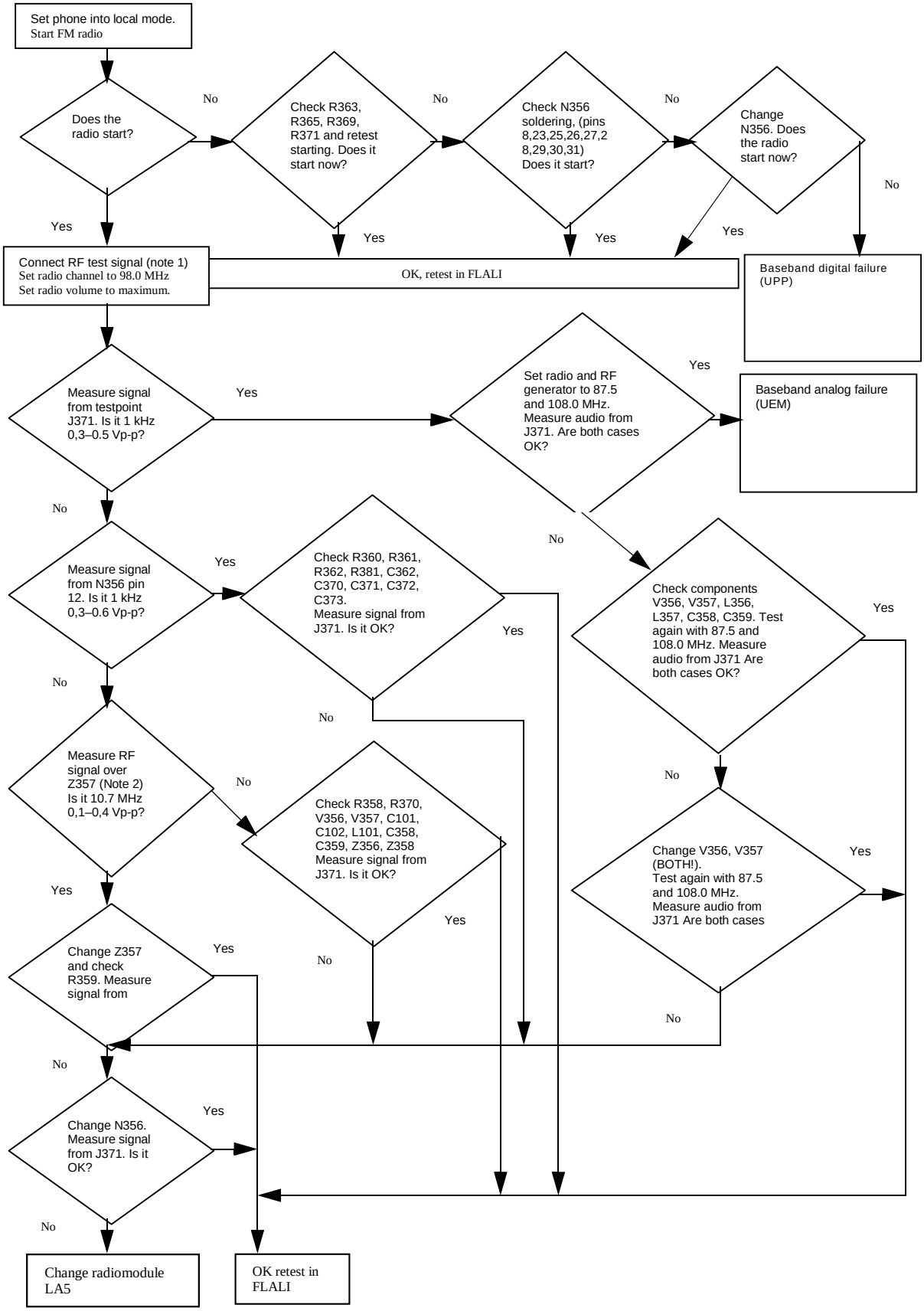
Notes to figure 2 "FM Radio troubleshooting diagram" on the next page:

Note 1. RF test signal parameters:

- Amplitude, *A*, –67.0 dBm
- Carrier frequency, f_c, 98,200 MHz
- Deviation, Δf, 75 kHz
- Modulating frequency f_m, 1,000 kHz (RF generator internal)

Note 2. Use 10x probe. Compare measured RF signal level to a known good product.

Figure 2: FM Radio troubleshooting diagram



RF Tuning and Calibration Instructions

Phoenix is used to control the phone.

TX tunings

When changing any TX components, all TX tunings need to be done.

Equipment needed for TX tuning:

- Spectrum analyzer
- Computer with Phoenix -software

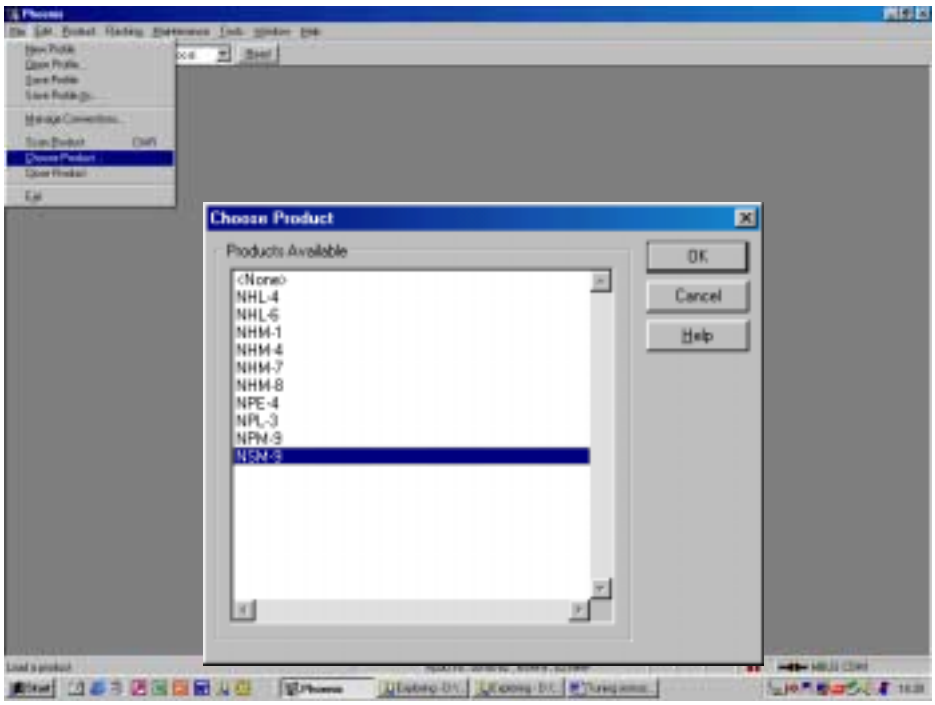
TX Output power tuning

Spectrum analyzer settings for TX output power tuning

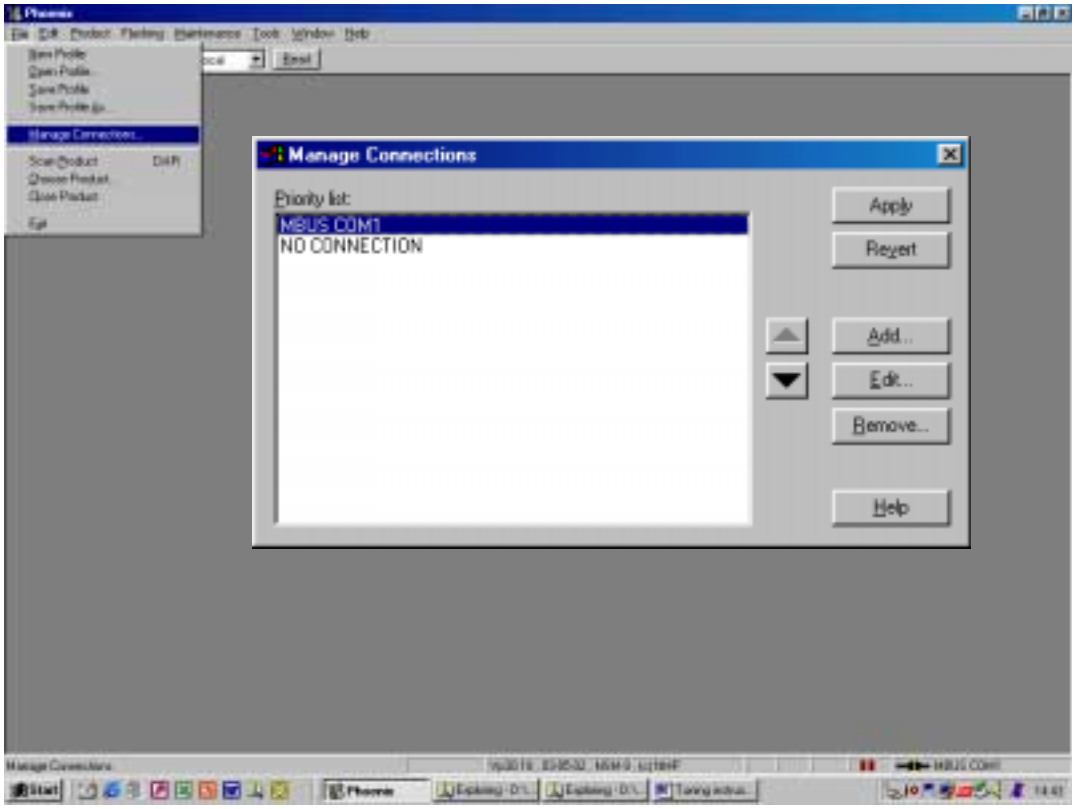
- Center Frequency GSM1900:1880 MHz
- Span: 0 Hz
- RBW/VBW: 3 MHz
- Sweeptime 5 ms
- Ref Level +30 dBm
- Trigger: Video

Note: Remember cable and test fixture attenuation.

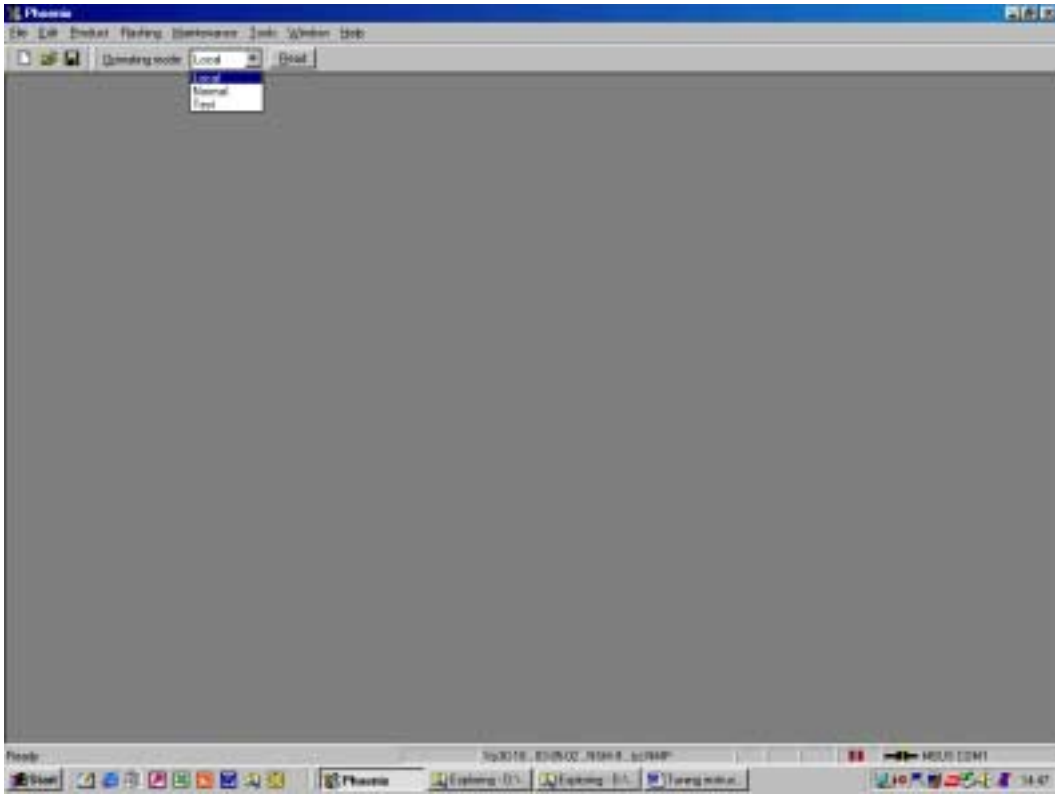
1 Start the Phoenix service software



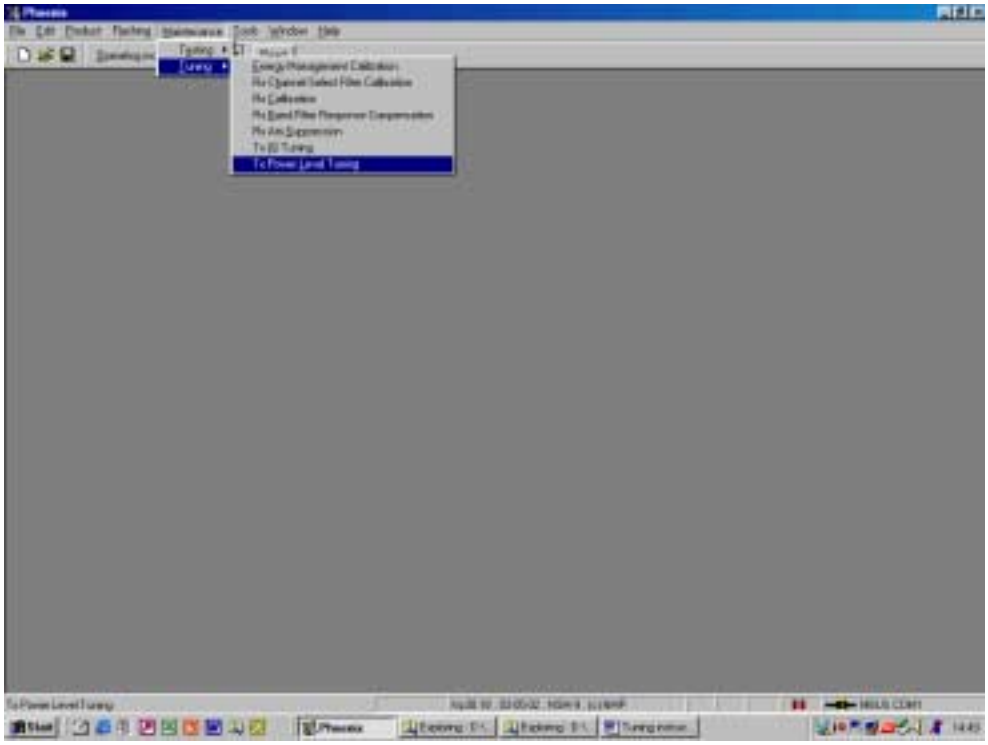
2 Scan product (Ctrl +R) should automatically detect NSM-9. If product is not found, choose product manually.



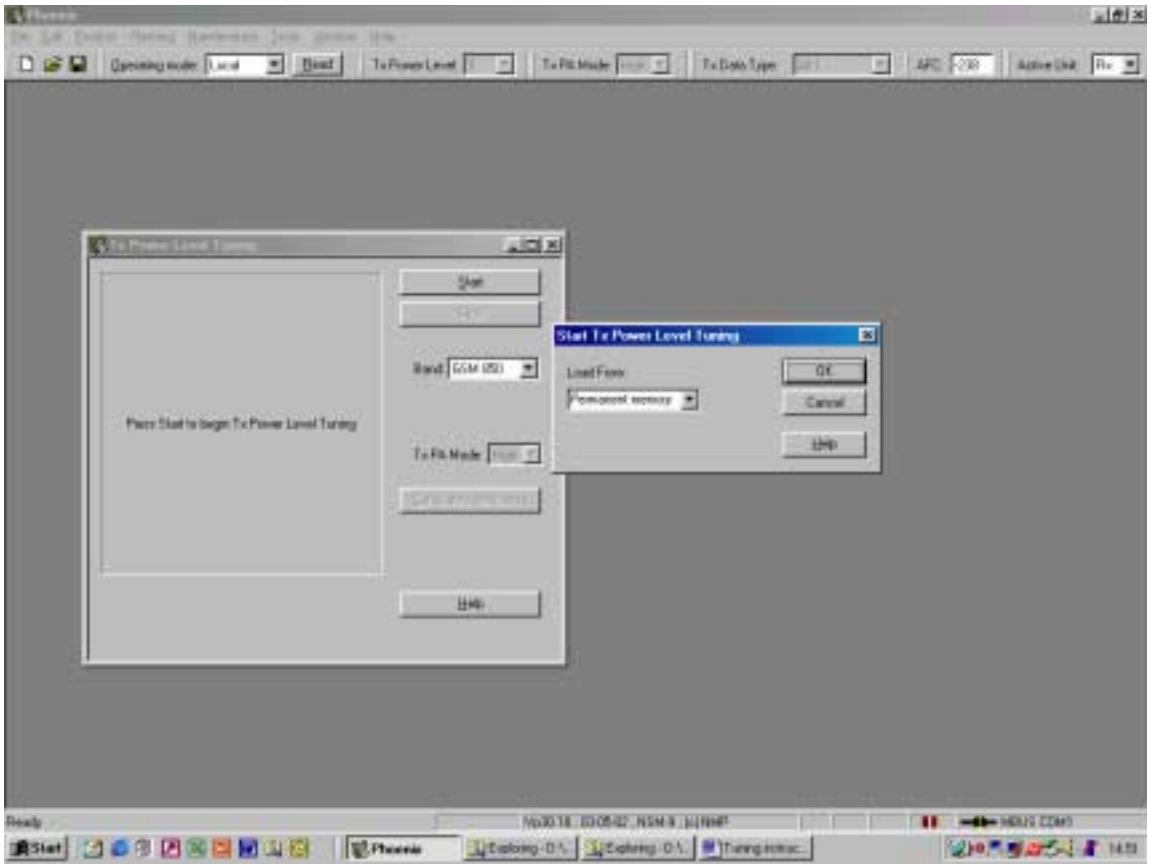
3 Phoenix should initialize connection automatically. If not initialize the connection manually for FILE –Manage connections -menu.



4 Change operating mode to Local:

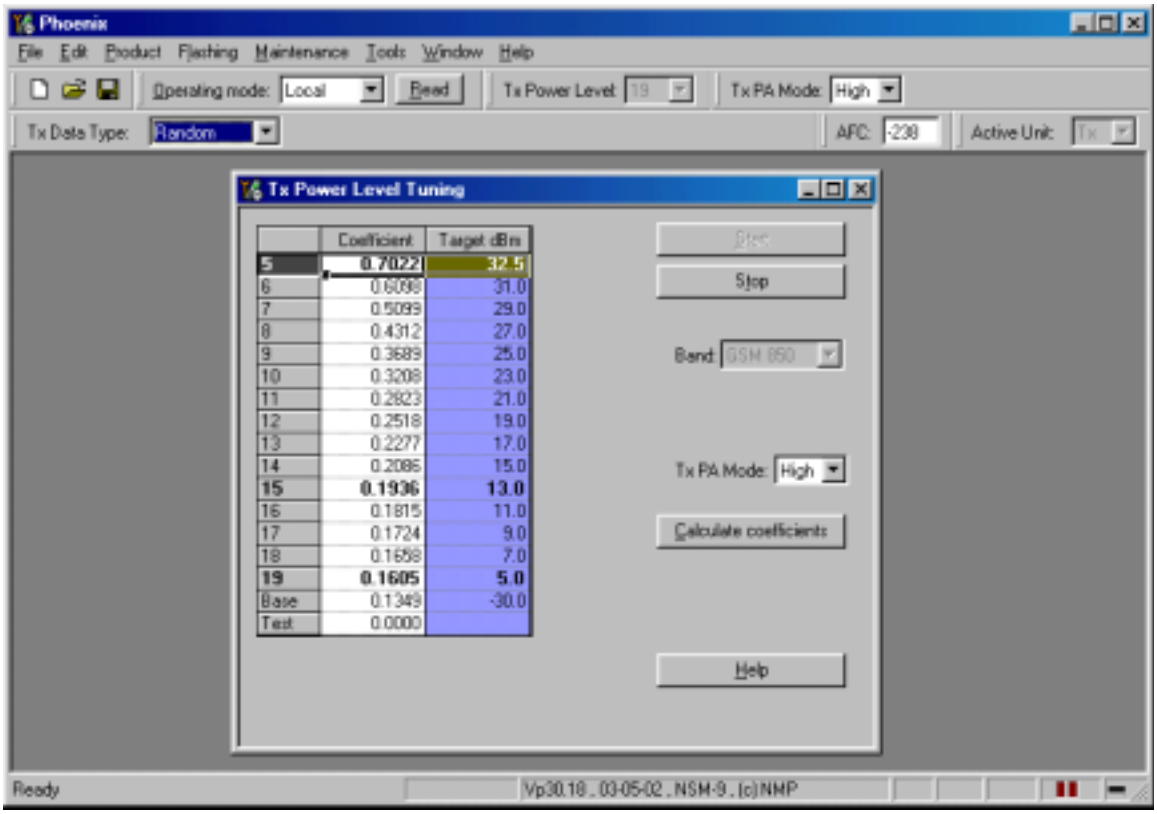


5 Select Tuning from maintenance – menu and choose TX power level tuning.



6 Select band GSM1900.

7 Press Start and load tuning values from Permanent Memory



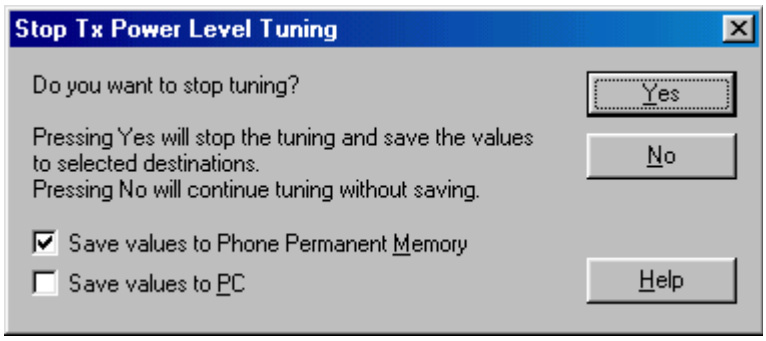
8 Adjust tuning values.

Note: It is only necessary to adjust Base (-30 dBm) PCL15, PCL 11 and PCL 0 in GSM1900. After that Calculate Coefficients – function can be used to linearize other values.

TX power tuning targets and limits:

GSM 1900 Power Level	Target power [dBm]	Tuning target tolerance	Testing limits
0	+29.5	+/- 0.1 dBm	+0.2 / -0.5 dBm
1	+28.0	+/- 0.5 dBm	+/- 1 dBm
2	+26.0	+/- 0.5 dBm	+/- 1 dBm
3	+24.0	+/- 0.5 dBm	+/- 1 dBm
4	+22.0	+/- 0.5 dBm	+/- 1 dBm
5	+20.0	+/- 0.5 dBm	+/- 1 dBm
6	+18.0	+/- 0.5 dBm	+/- 1 dBm

7	+16.0	+/- 0.5 dBm	+/- 1 dBm
8	+14.0	+/- 0.5 dBm	+/- 1 dBm
9	+12.0	+/- 0.5 dBm	+/- 1.5 dBm
10	+10.0	+/- 0.5 dBm	+/- 1.5 dBm
11	+8.0	+/- 0.5 dBm	+/- 1.5 dBm
12	+6.0	+/- 0.5 dBm	+/- 1.5 dBm
13	+4.0	+/- 0.5 dBm	+/- 1.5 dBm
14	+2.0	+/- 1.0 dBm	+/- 2.0 dBm
15	0	+/- 1.0 dBm	+/-2.0 dBm
Base	-30.0	+/- 2.0 dBm	+/-2.0 dBm



9 When tuning values are correct, save them to Phone Permanent Memory

New tuning values will be in use immediately.

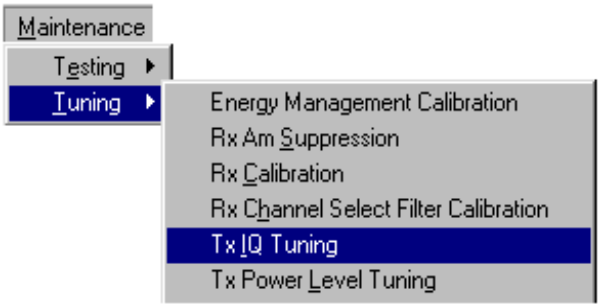
10 Close TX tuning window

TX IQ tuning

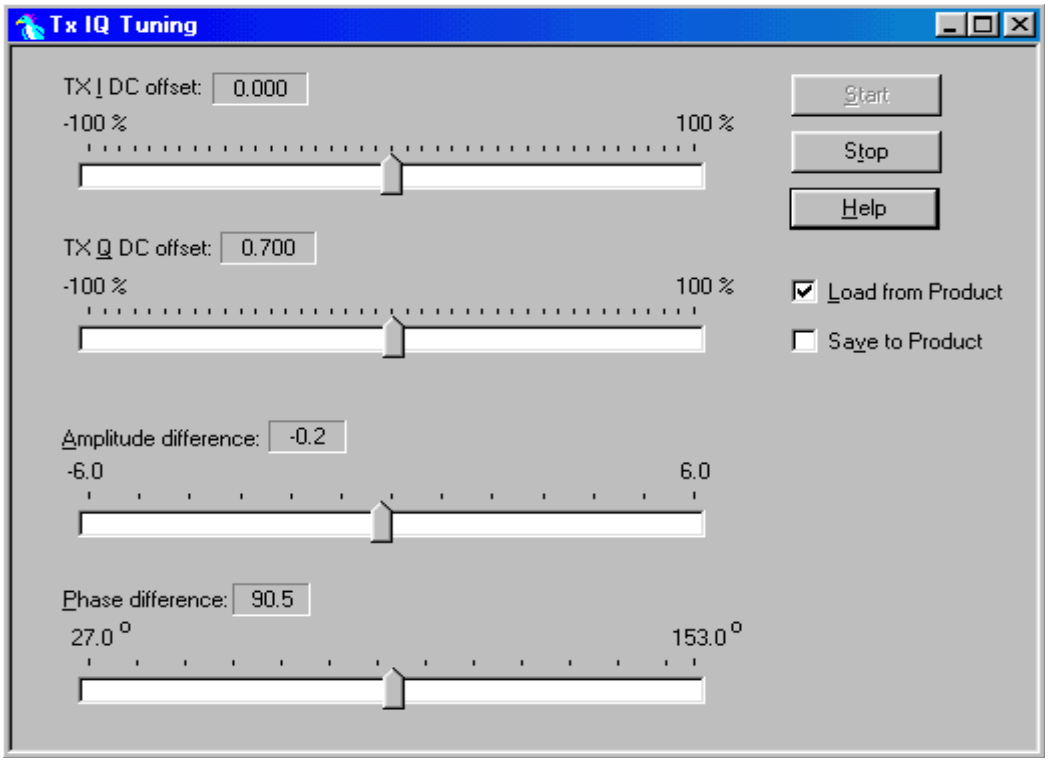
Spectrum analyzer setting for TX IQ tuning:

- Frequency: 1880MHz
- Span: 200kHz
- RBW/VBW: 10kHz
- SweepTime: 2s
- RefLevel: +20dBm

1 Select **Tuning** from Maintenance –menu bar and choose **TX IQ Tuning.**

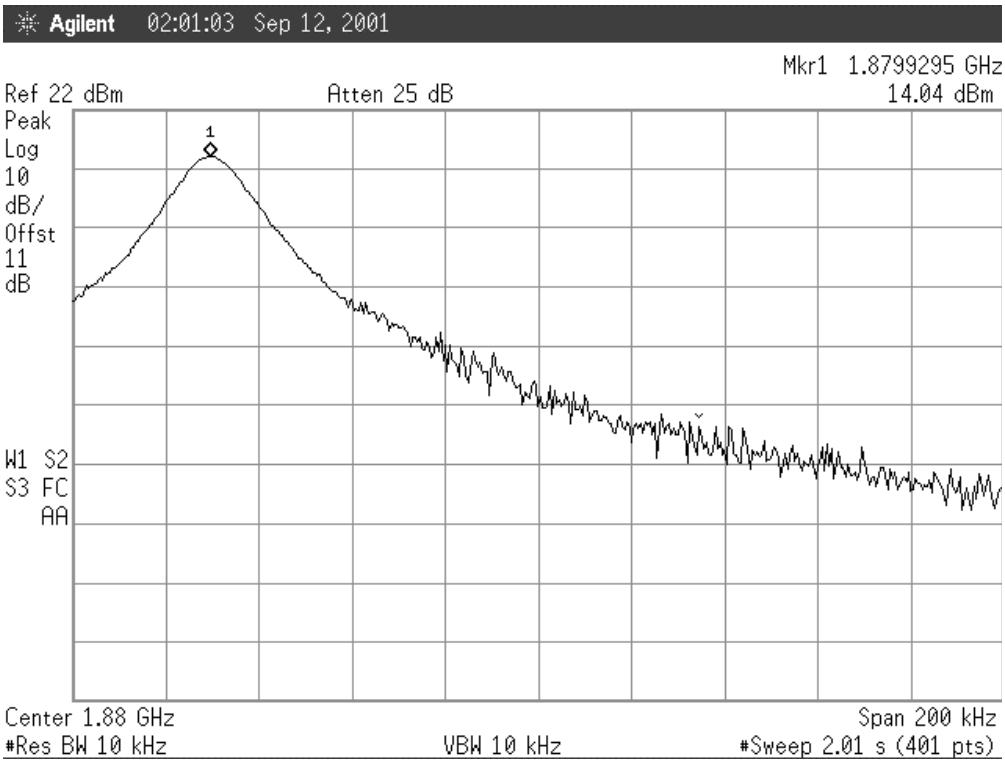


2 Load tuning values from Product and **Start** –tuning.



Adjust tuning values so that IQ spectrum is balanced (see example picture below, data ‘

All 1').



3 Choose **Save to Product** and **Stop** tuning.

--> Close **Tx IQ Tuning** window.

RX tunings

When changing any RX components, all RX tunings need to be done.

1 Channel select filter

2 RX tuning GSM1900 (gain step A1 ... A9 tuning)

3 AM suppression GSM1900 (to minimize AM signal disturbance)

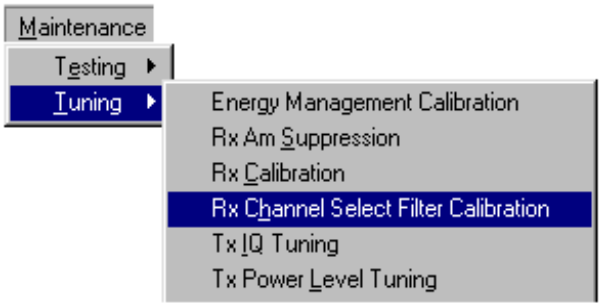
Equipment needed for RX tuning:

- Signal generator with AM-Modulation
- Computer with Phoenix -software

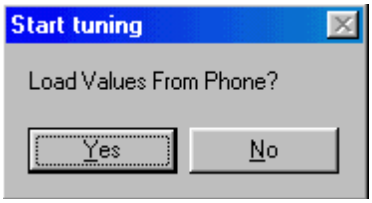
Channel select filter calibration

1 Choose product and initialize connection as in TX output power tuning procedure (Steps 1 and 2)

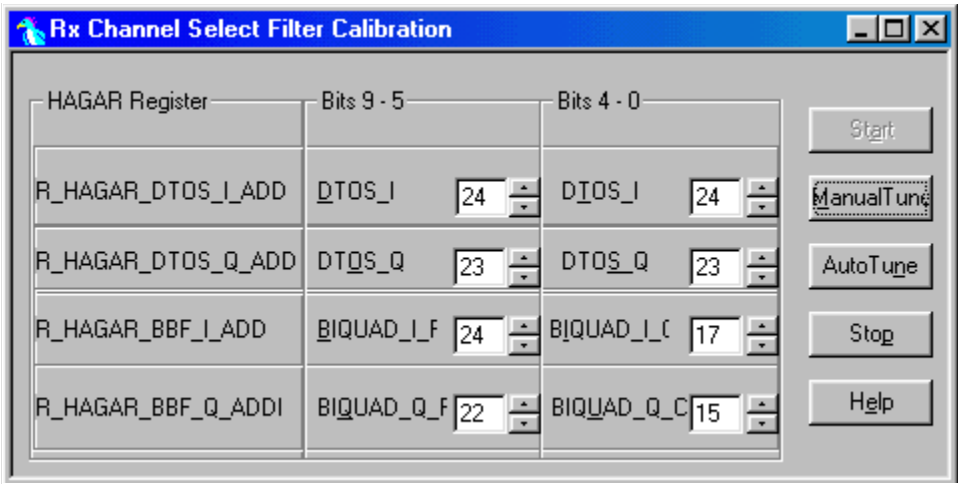
2 Select **Tuning** from Maintenance –menu bar and choose **RX Channel Select filter Calibration.**



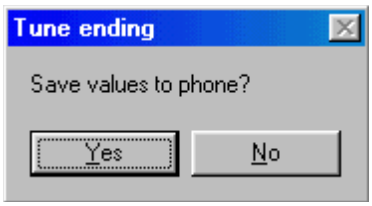
3 Load tuning values from phone.



4 Use **Auto Tune** to calibrate Channel Select filter.



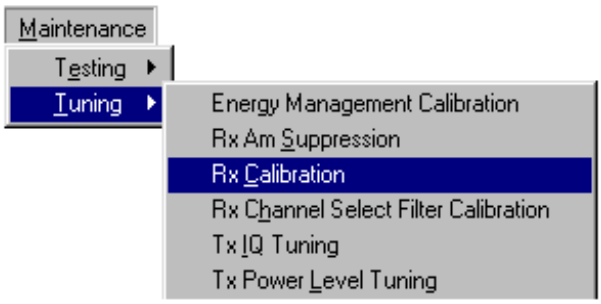
After tuning, select **Stop** and save the values onto the phone.



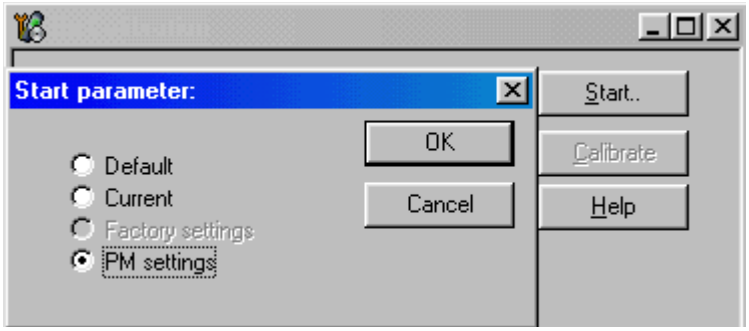
5 Close the **Rx Channel Select Filter Calibration** window.

RX tuning GSM1900

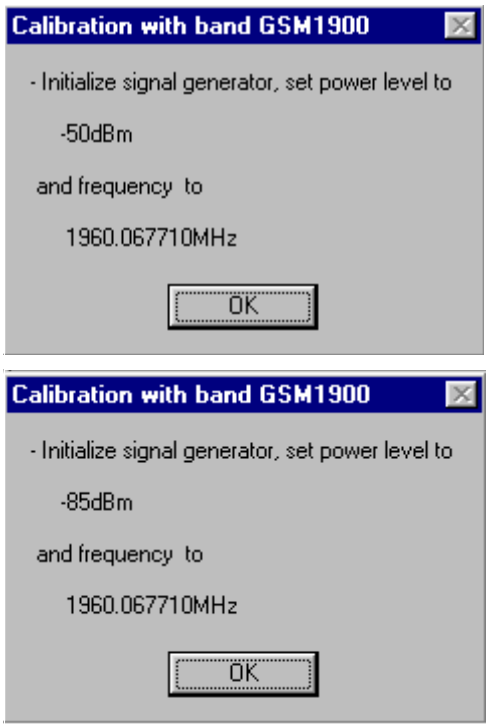
1 Select **Tuning** from Maintenance –menu bar and choose **RX Calibration.**



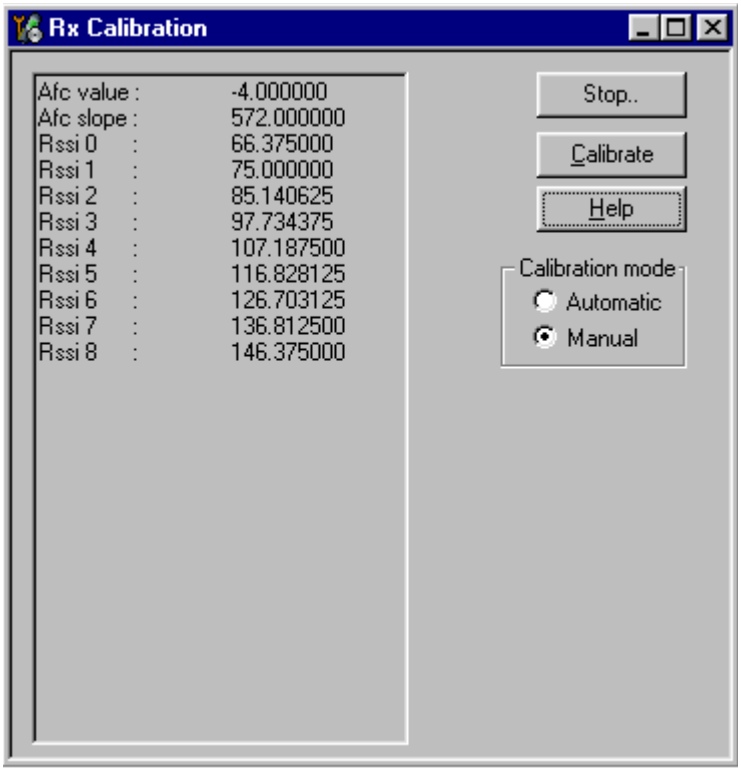
2 Start **Manual tuning** with **PM Setting.**



3 Choose **Calibrate** and adjust signal generator accordingly.



4 **Stop** and **Save** new calibration values to phone.



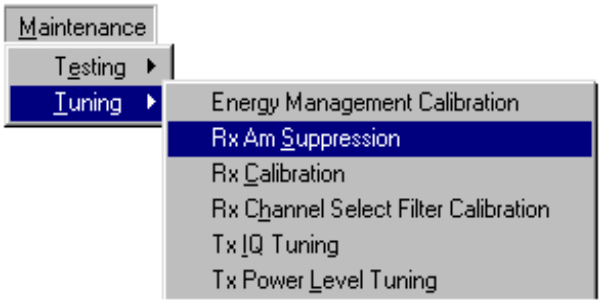
--> Close **Rx Calibration** window.

RX Calibration limits:

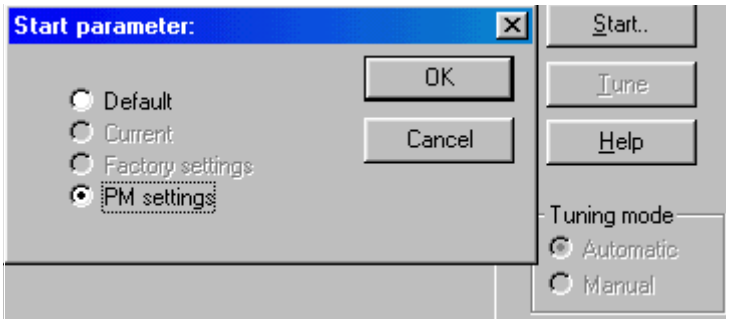
RSSI 0	60	70
RSSI 2	70	80
RSSI 3	80	90
RSSI 4	90	100
RSSI 4	100	110
RSSI 5	110	120
RSSI 6	120	130
RSSI 7	130	140
RSSI 8	140	150
Check AFC_slope	0	1000
Check AFC_value	-500	500

AM suppression tuning

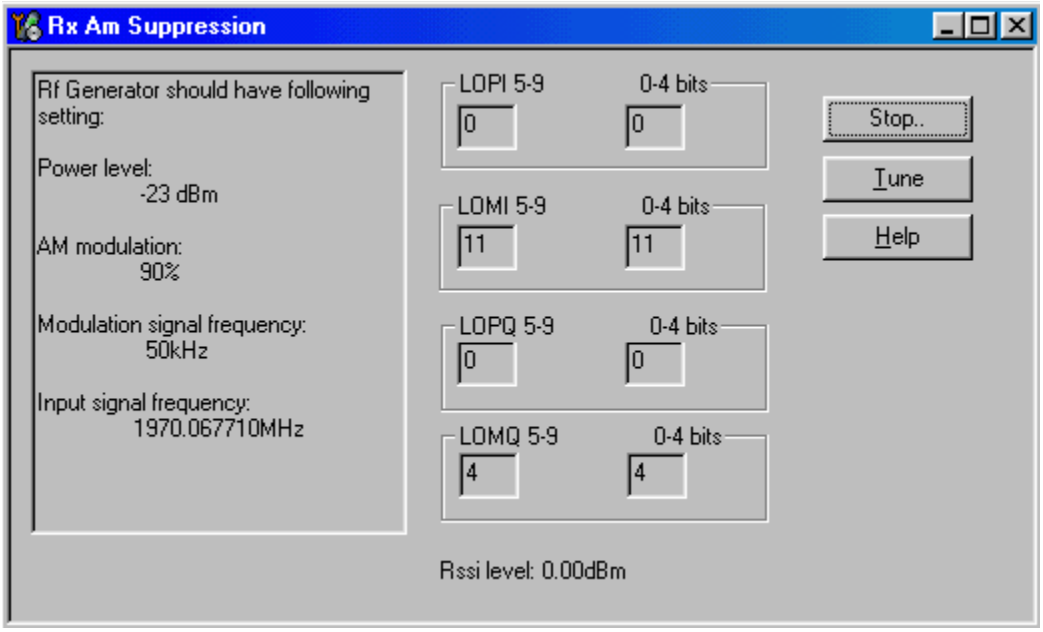
1 Select **Tuning** from Maintenance –menu bar and choose **RX Am Suppression.**



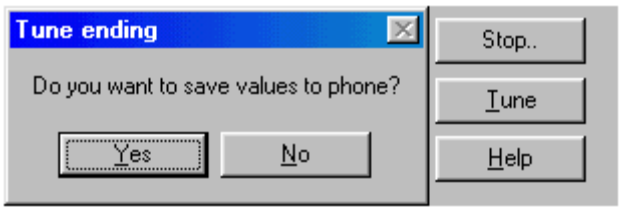
2 **Start** tuning with **PM settings.**



3 Adjust signal generator accordingly and **Tune.**



4 **Stop** and save values to phone.



--> Close **Rx Am Suppression** window.

Rx Am Suppression limits:

LOP_I	0	1023
LOM_I	0	1023
LOP_Q	0	1023
LOM_Q	0	1023
RSSI	-120	-92

RF Service Tools

MJS-46 Module Jig

All RF tunings should be performed in MJS-46 Jig. When using Test Jig MJS-46, the reference level attenuation is 0.1 dB + cable loss.

JVB-1 Docking Station, MJF-6 Adapter and coupler CPL-9

The reference level attenuation for Docking Station JBV-1 + MJF-6 adapter with antenna coupler CPL-9 is approximately 4 dB +cable loss.There can be minor differences between CPL-9 antenna couplers, but maximum distribution is +-0.3dBm. Attenuation can vary between antenna couplers. There is differences in attenuations between low and high channel, but those can be ignored.

Coupler attenuation calibration

When Docking Station with MJF-6 and CPL-9 inside the shield box JSX-1 is used, then calibration procedure is following:

- Measure one known phone in **MJS-46 Module Jig** in Ch 661, the output power **(P1)** should be 29.5dBm +- 0.2dB. Remember the jig loss 0.1dB and cable loss.
- Assemble the measured phone in to mechanics
- Put the phone in to the JBV-1 Docking Station, without **JXS-1 Shield Box**
- Measure the output power **(P2)** in Ch 661
- The attenuation **(A1)** of the antenna coupler is: A1=(P1+0.5dBm)-P2
- (**Note!** Mechanics will increase output power 0.5dB)

Typical coupler (CPL-6) attenuation is 4.0dB. If measurements are done without **JXS-1 Shield Box**, the same value can be used in TX and RX.

If using shielded box **JSX-1**, additional loss is needed separately for LO, MID and HI Channels. Typical loss values are: LO= 5.7dB, MID=2.3dB and HI=0.5dB

Functionality Testing Limits

When checking the phone's functionality in the JBV-1 docking station with a coupler, the TX power may vary to some degree. TX power levels 14 and 15 should be ignored, as the coupler's response is not reliable. The following table lists the TX output power tolerances, when CPL-6 is used for measuring:

Table 1: TX Output Power Tolerances

PCL	Target (dBm)	Tolerance (dBm)
0	29.5	+/-3
1	28	+/-3
2	26	+/-3
3	24	+/-3
4	22	+/-3
5	20	+/-3
6	18	+/-3
7	16	+/-3
8	14	+/-4
9	12	+/-4
10	10	+/-4
11	8	+/-4
12	6.5	+/-4
13	5	+/-4
14	3.5	+/-5
15	2	+/-5

JXS-1 Shield Box

Metal shielded box, mentioned to avoid disturbing RF signals, has a great effect to TX output power, Bit error and Signal Strength reporting results, since the surface of shielded box is reflecting RF-waves and therefore changing RF performance.

In following pictures the behavior of JVB-1 Docking Station with MJF-6 adapter is presented in JXS-1 Shield Box and without the box (coupler).

The measurements are done in the following conditions:

- Temperature +25 °C (77 °F)
- NOKIA 6590 Cellular Phone
- NOKIA JXS-1 Shield Box
- NOKIA JBV-1 Docking station with antenna coupler (1900 MHz)
- RF-Attenuation for MJF-6 and cable is 4.5dB

Figure 3: Power 30 dBm

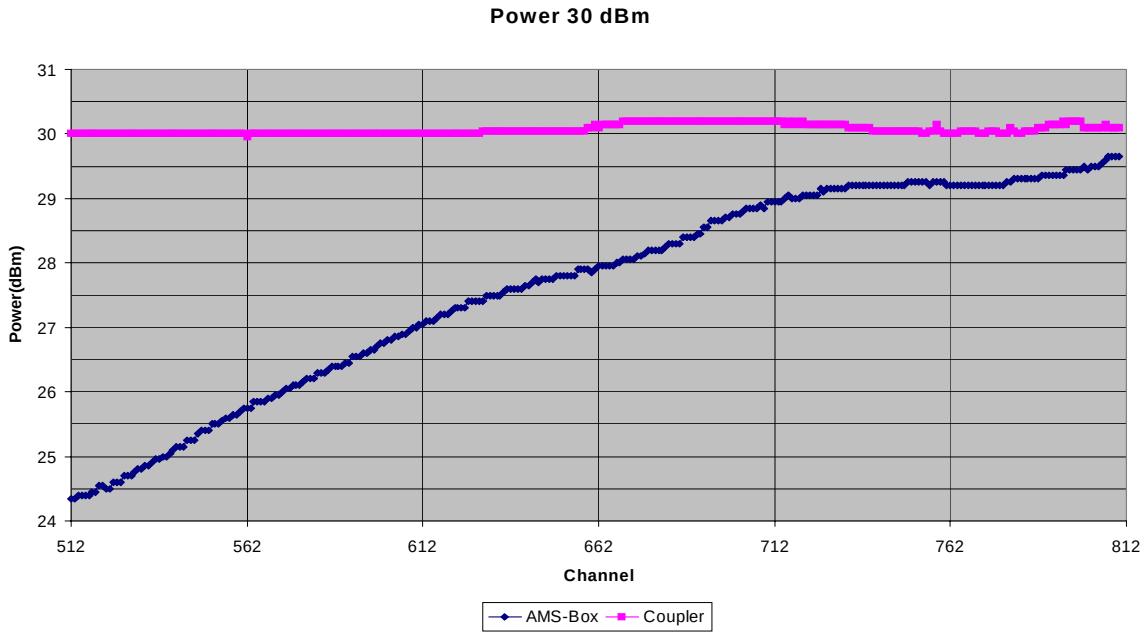


Figure 4: Phase error RMS

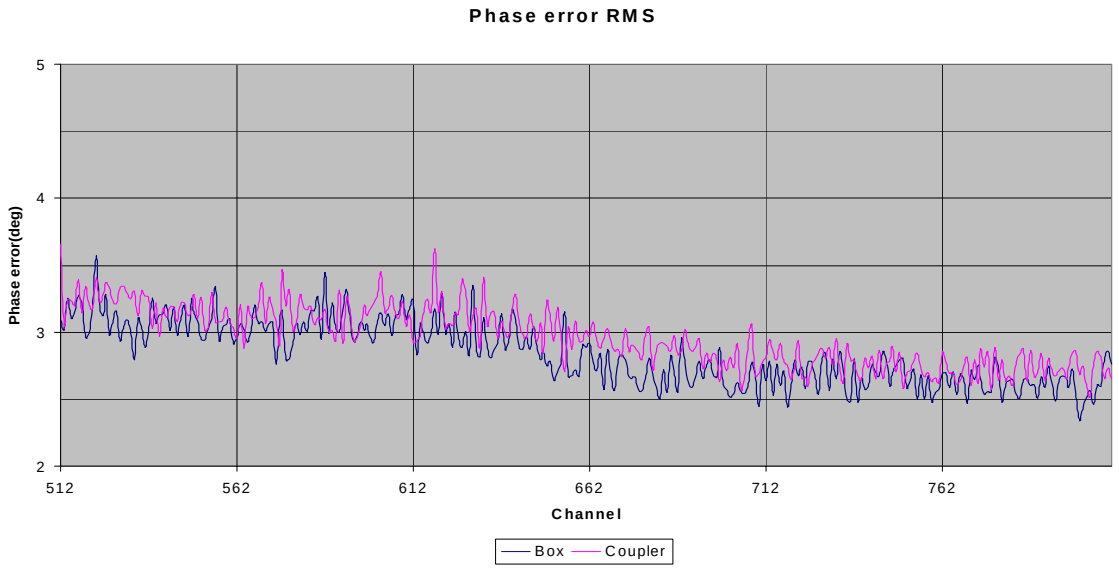


Figure 5: Signal Strength Reading

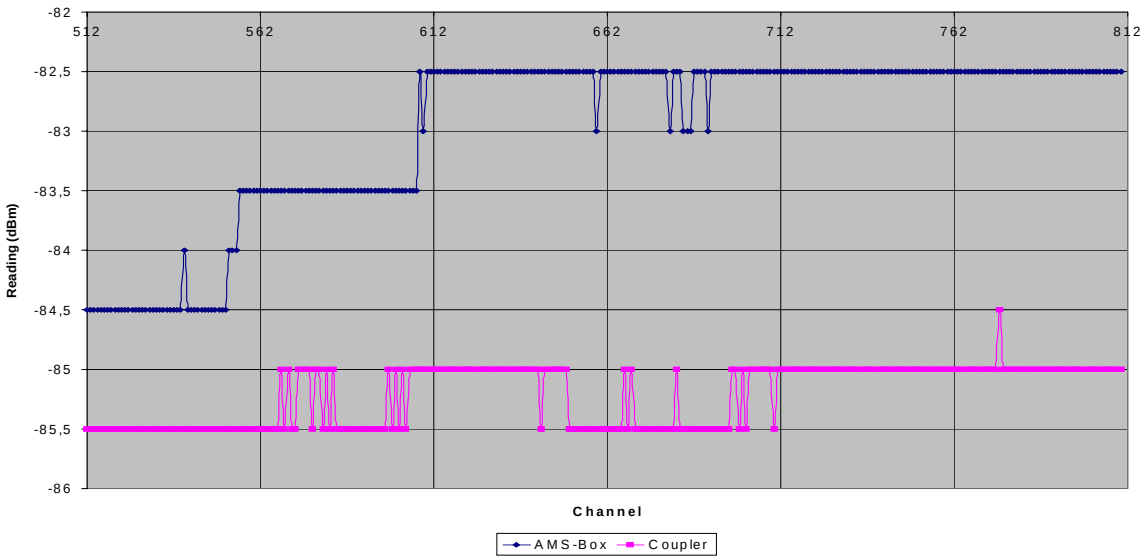
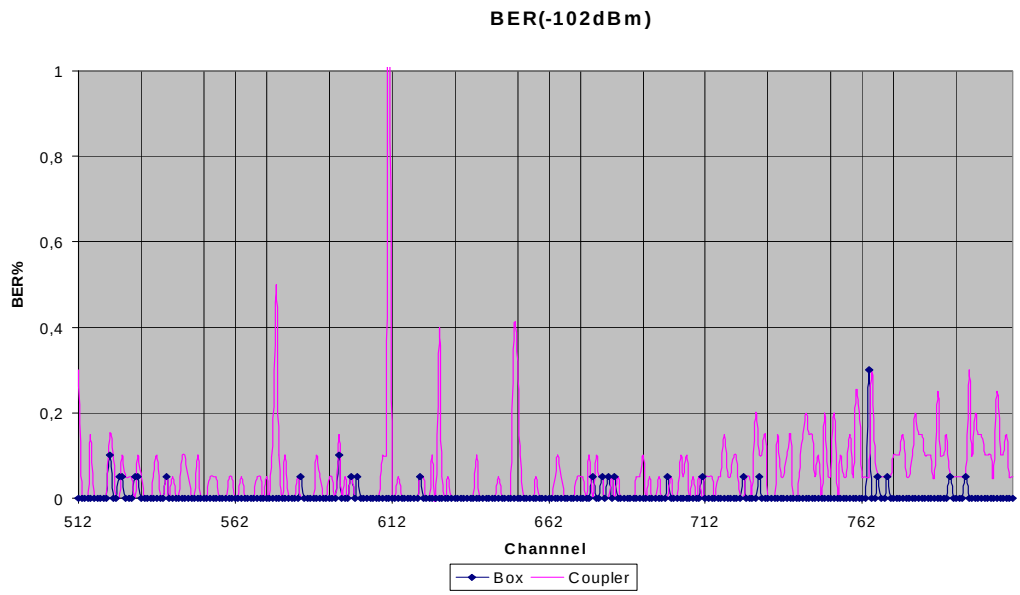


Figure 6: BER(-102 dBm)



When using JXS-1 shield box different RF attenuations have to be used. It is recommended that in the shield box all measurement are performed only on **channel 661** and additional 2.5 dBm loss in added to Reference level offset, so that total RF attenuation caused by JXS-1 shield box and CPL-6 Adapter is **6.5 dBm+ cable loss**.